DIGIGRAPHIC

MAN ⬌ MACHINE

SYSTEMS

DIGIGRAPHIC SYSTEM 270

SYSTEM INFORMATION MANUAL

CONTROL DATA

CORPORATION

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DIGIGRAPHIC SYSTEM 270

SYSTEM INFORMATION MANUAL

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CONTROL DATA CORPORATION
Digigraphic Laboratories
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SECTION 1
INTRODUCTION

The Control Data Corporation's Digigraphic System represents a recent and significant refinement of certain well established techniques for implementing man-machine communications through use of a Cathode Ray Tube and light sensory feedback. During the evolution of modern digital computer systems, a vast range of technological problems have been resolved to the extent that today's machines have capabilities not even conceived of a decade ago. As a result of this continuing technological improvement, computer system research has tended to focus more and more on the need to refine the basic concepts of man-machine communication.

A technological paradox currently exists wherein the unit cost per computer instruction executed has been reduced to an extremely low level, yet this potential is being fully realized in only the most specialized areas. This tendency toward specialized application has been a direct result of the unreceptiveness of computers to human methods of communication. Thus, the tasks most frequently performed by the computer have been those readily formulated in the abstract language of computers.

Full use of the general-purpose nature of digital computers requires an interface whereby human and computer languages become mutually compatible. The purpose of the Digigraphic System is to provide that interface. With this system, graphic information is entered by the Digigraphic System directly, in digital form, into the central computer as the graphic data is being delineated by the user on the display screen. The graphic input is immediately available for automatic processing by the central computer under operator control. The results of the specified graphic data processing is immediately displayed in a flicker-free manner.

The modular design of the Digigraphic System readily provides for multiple console configurations plus operation of remote consoles. The Digigraphic display technique requires minimum interruption of the central computer. A buffer memory supplies display data to consoles for an off-line display. The computer is utilized only to process short bursts of display

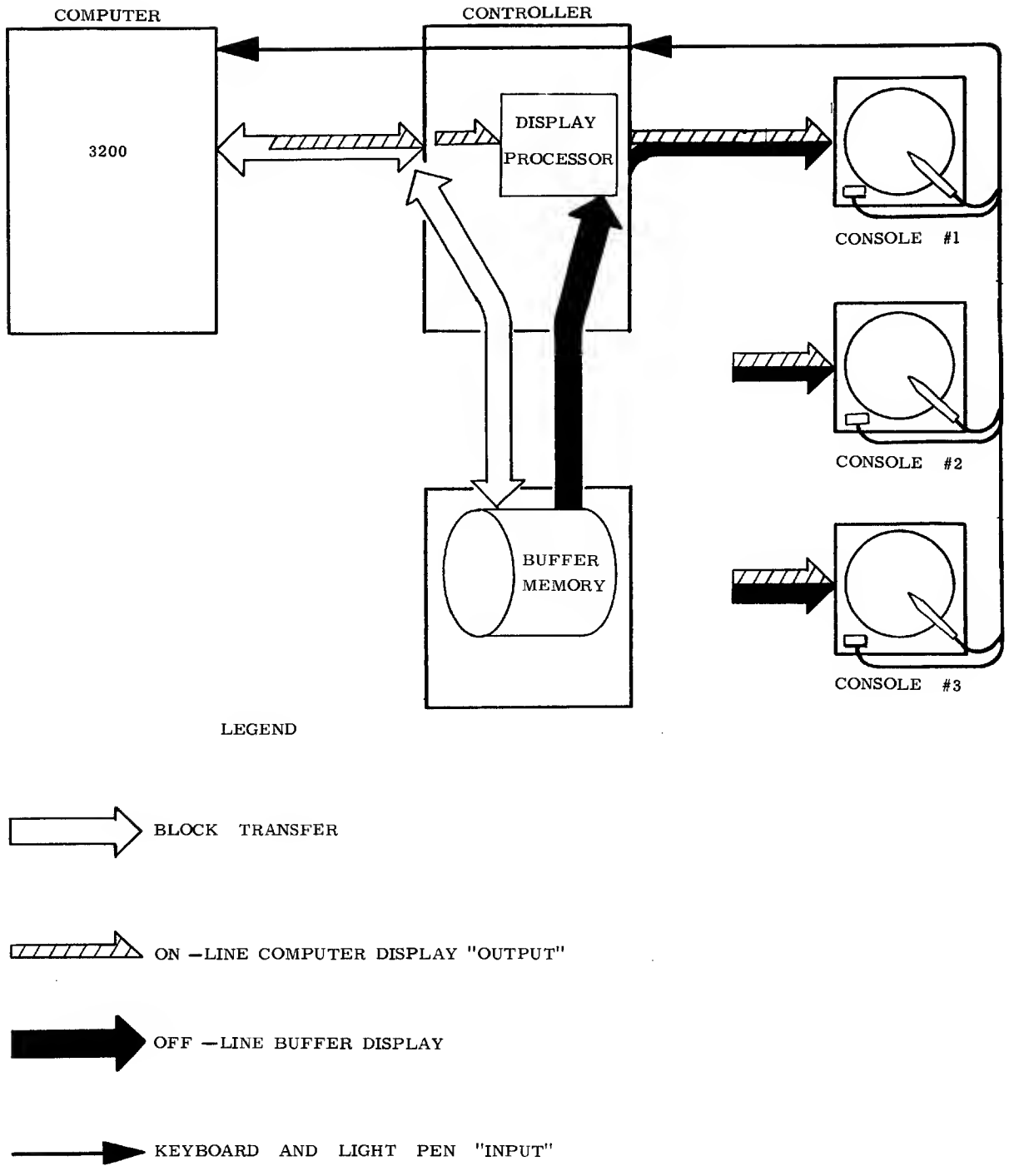


Figure 1-1 Computer/Buffer Memory Display

change information thereby maintaining a continuous graphic display on a true off-line basis (refer to Figure 1-1). The expandability features of the system are based on a new concept wherein system control and equipment interfaces are accomplished by macro-programming techniques. The result is a unified operational system permitting a whole new approach to digital system application.

The real-time mode of Digigraphic operation (demonstrated in Figure 1-2), in conjunction with the off-line display feature, provides a powerful vehicle for effective man-machine communications and economic implementation of massive graphic information storage and retrieval systems.

The design philosophy of the Digigraphic System is based on the fundamental requirement that system controls and operational characteristics of a specific installation are defined by the user's supplementary applications-oriented programs. This philosophy is implemented by allocating complete system control to the Digigraphic System Executive Programs.

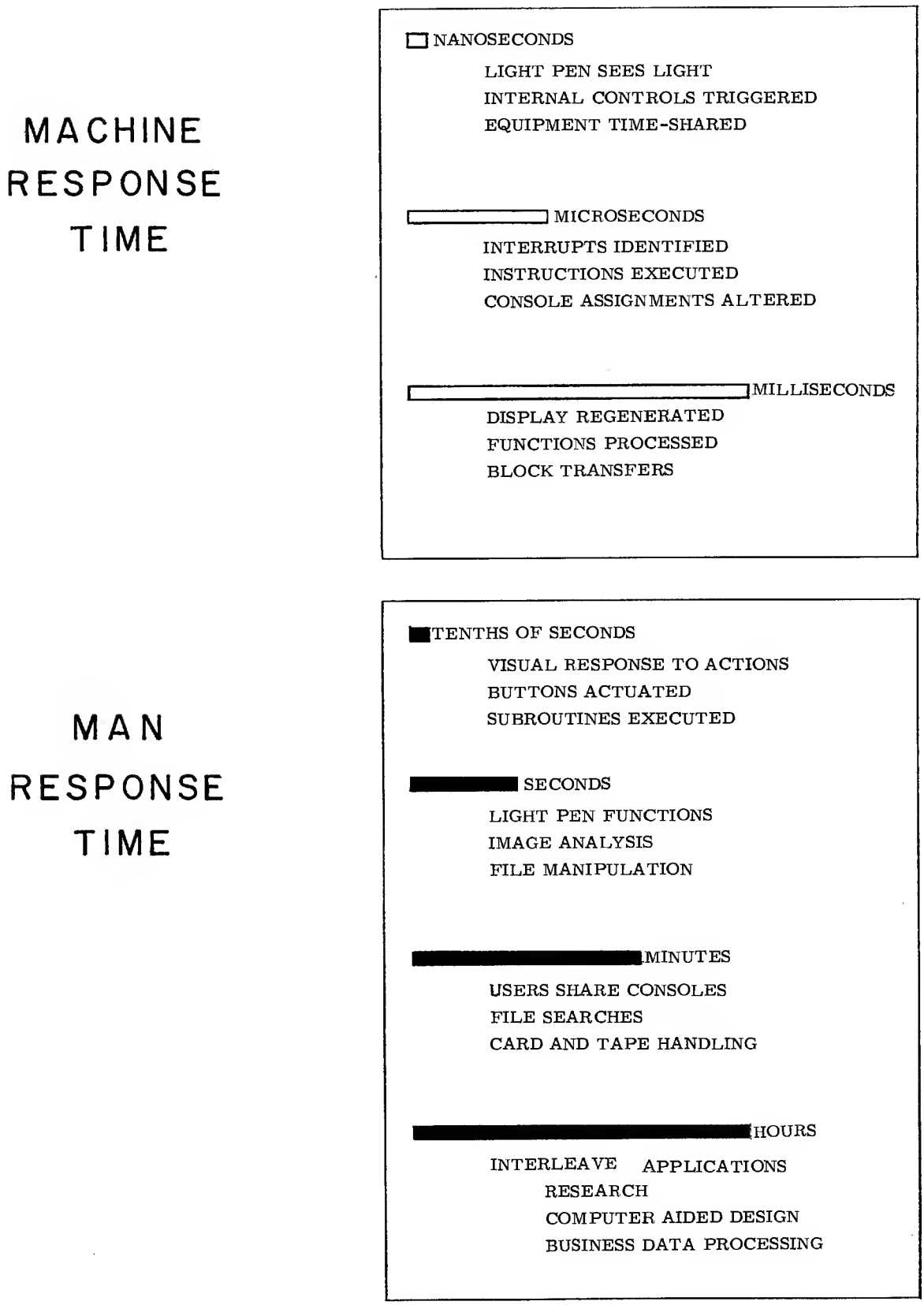


Figure 1-2 Digigraphic System Response Time

SECTION 2
GENERAL DESCRIPTION

The primary Digigraphic components are a controller, buffer memory and up to three consoles. These units in conjunction with the prescribed computer configuration comprise the basic Digigraphic System (Refer to Figure 2-1). The Digigraphic System is compatible with the CDC 3200 System I/O interface. Full Digigraphic operational capability is achieved through the use of the conventional 3200 computer instruction repertoire including the conventional I/O instructions.

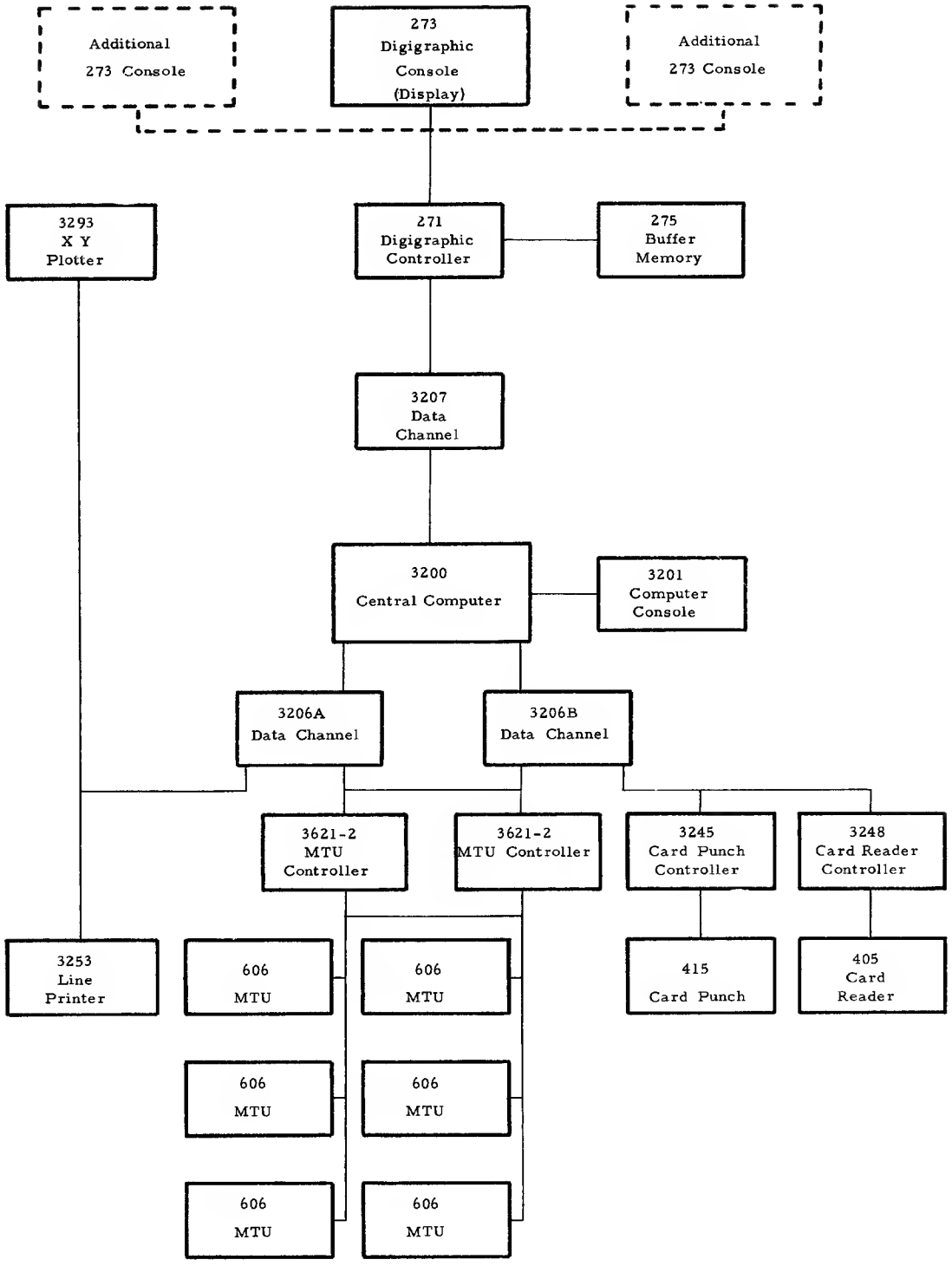
MODEL 271 DIGIGRAPHIC CONTROLLER

The Digigraphic 271 Controller contains the logic necessary for compatibility with a 3200 Computer. The unit interprets system data and is capable of transferring information from the computer to any one of three consoles or to buffer memory. This communications link is also two-way, since a read instruction or a write instruction can be executed by the 3200 Computer so as to address the controller which in turn will address one of the four units assigned to it.

The controller utilizes one cable for 60-cycle, 115-VAC, 3-wire input power, one 400-cycle, 208-VAC 5-wire power cable and two 29-pair logic cables that are used to interface with the 3200 Computer. The controller receives terminator power from the 3200 Computer and distributes one terminator power line to each of the three consoles. The controller connects to each console with two 29-pair logic cables. The unit also has five 29-pair logic cables which connect to buffer memory. The controller utilizes a standard Control Data power supply for +20-volts dc, and -20-volts dc. Each console connects to the controller by the two above mentioned logic cables.

MODEL 275 DIGIGRAPHIC BUFFER MEMORY

Buffer memory is a magnetic drum memory device which receives input power from a 60 cycle 208-VAC 5-wire cable and is connected to the controller through five logic cables. Three of these cables are used to provide output logic signals for six head bands, with each head band comprised of 12 data-bits plus a parity bit. The fourth cable provides 13 write-lines



Configuration at Digigraphic Laboratories, Burlington, Mass.

Figure 2-1 Typical Digigraphic System

plus necessary timing signals to synchronize the controller with buffer memory during drum write operations. The fifth cable carries the various clocks which synchronize the read and write operations and control the timing cycle of the controller. The buffer memory is contained in a standard peripheral controller cabinet, and provides approximately 1.56 million bits of storage or 120,000 bytes (a byte comprises a 12-bit word). The method of recording is phase modulation with a bit density of 345 bpi.

Separate read-write amplifiers are provided for each head band to accomplish simultaneous reading and writing. One set of these write circuits accommodates a head band. A head band consists of 12 tracks of data plus a parity track; 12 data bits (one byte) plus parity are written in parallel on the drum surface during a drum clock period. The computer can write on only one of the 6 drum head bands at any one time (Figure 2-2). All 6 head bands are read simultaneously to provide the console displays. The 6-band output is coupled to the controller for selection by the consoles. A console is connected to only one head band at any one time. Section 3 of this manual explains how a particular head band is selected for console display.

Each head band is divided into 16 addressable sectors. Each sector can store 1250 bytes of information.

Buffer memory provides for storage of display identification and control information produced by the Digigraphic program in the central computer. When graphic inputs are entered into the central computer, the Digigraphic System program produces compact descriptions of the graphics being generated, converts the data to display instructions, and stores the instructions in buffer memory. These instructions contain such information as brightness control, on-off control, changes in beam direction and byte scaling. Display instructions may be selectively read off the drum in the proper sequence and routed to one or more consoles for immediate display. The display memory rotates at a rate of 30 revolutions per second to produce a display frame rate of 30 frames per second. Display drum areas not assigned can be used as a general purpose memory for the central computer.

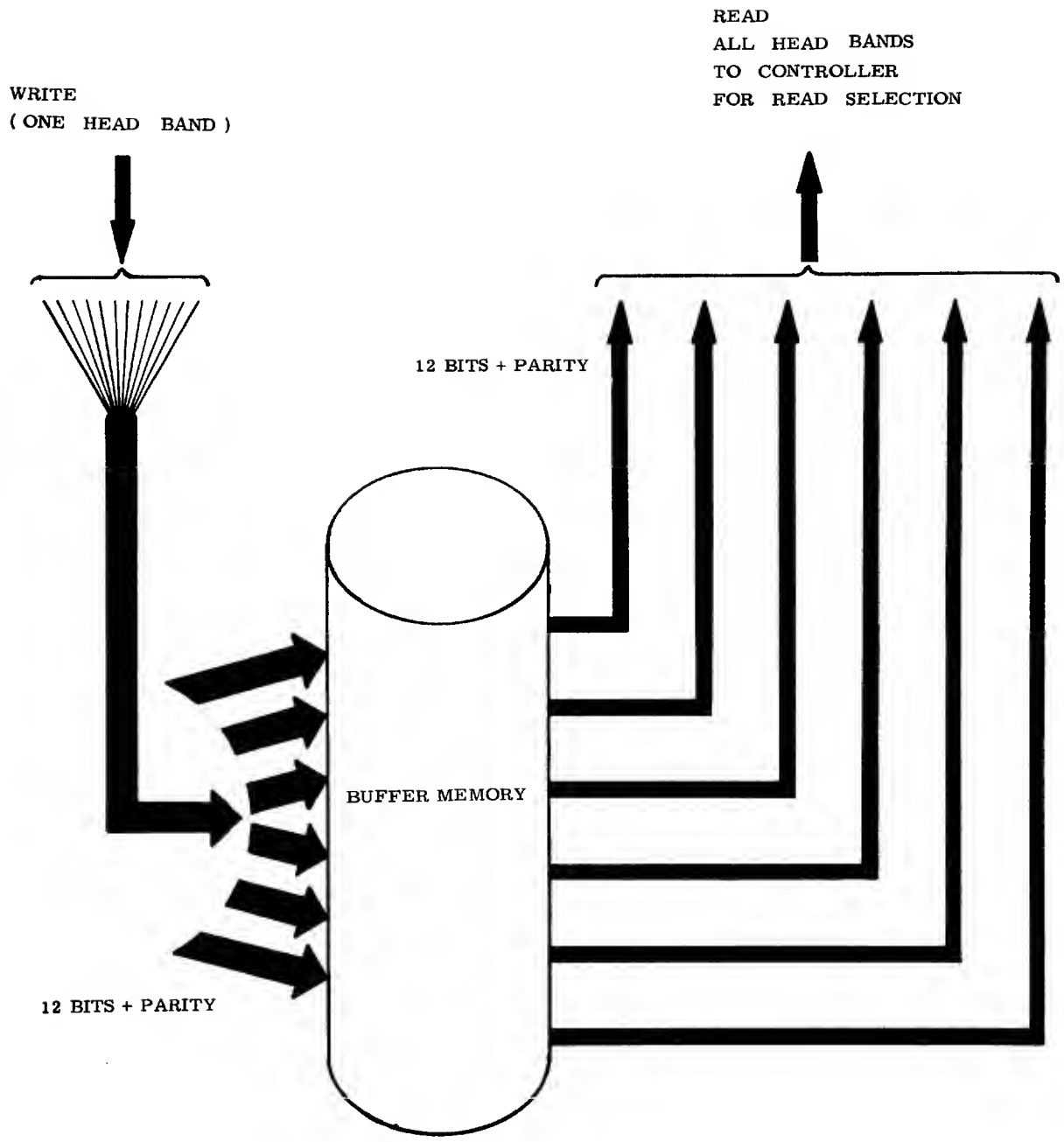


Figure 2-2 Buffer Memory Head Bands

MODEL 273 DIGIGRAPHIC CONSOLE

The 273 Digigraphic Console (Figure 2-3) is the input/output and human control center for the Digigraphic System. The complete range of system graphic capability can be controlled from the console without recourse to other control points. The console is designed for maximum operator utilization and comfort and can be used efficiently at normal room light levels.

The console cabinet is a desk size unit which mounts a rectangular housing assembly off-centered to the left providing desk space to the right. The housing assembly contains a magnetic shield and a 22-inch diameter CRT centered on the front panel housing. The housing assembly retracts into the console and is manually adjustable. The range of adjustment allows the tube face and front panel to be moved through approximately 60-degrees of slope at increments of 10 degrees starting 15 degrees off the horizontal.

A set of switches along the top rim of the housing assembly panel are used to control system start-up and shut-down. The housing assembly panel also secures the light pen flexible fiber optics pipe and serves as a platform for positioning the magnetically secured keyboard. Two quick-disconnect plug receptacles are located on the housing assembly front panel, one on each side of the CRT, for attaching the keyboard flexible cable.

The 22-inch CRT is a precision, 52-degree, high-resolution unit having a nearly flat display face to minimize parallax error. The CRT is protected with an implosion shield furnished with an anti-reflective finish. The display face is coated with P-7 phosphor which is deposited in two layers. One layer produces blue-violet light with short persistence to facilitate light pen tracking. The other layer reacts with yellow-green light having considerably longer persistence to minimize flicker. With a continuously rewritten display the light from both phosphor components combine to appear light blue to the human eye.

The deflection yoke and driving circuitry is designed to provide a full 52-degrees of beam deflection to permit addressing of the complete display area. As a result 4096-points on the X-axis and 4096-points on the Y-axis are addressable.

A 14-inch by 14-inch square or an 11-inch by 17-inch rectangle may be reserved on the 20-inch display surface for the precision construction of graphic data. If so, the segments on the periphery of this square or rectangle

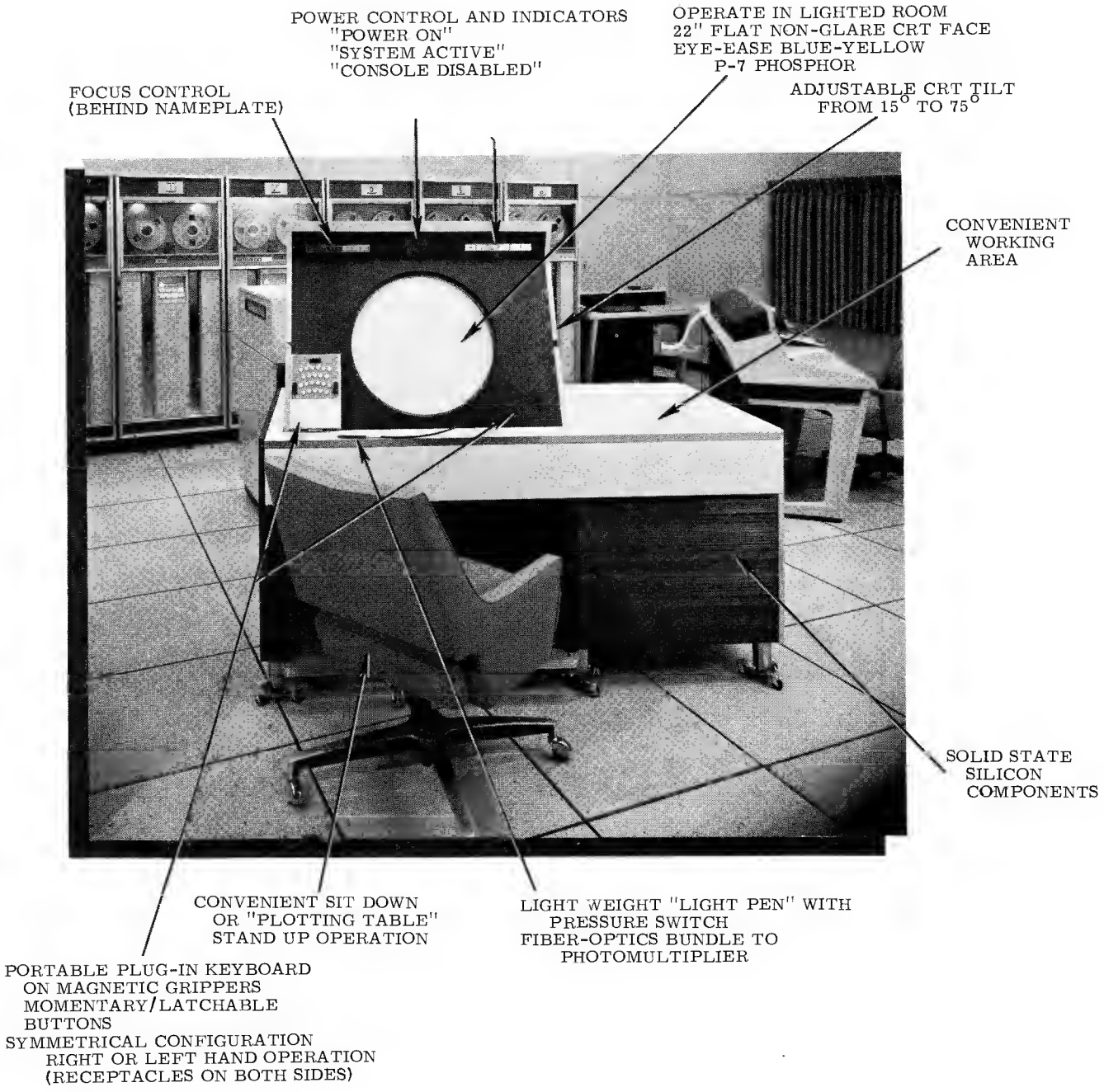


Figure 2-3 Digigraphic Console

may be used for a variety of functional displays such as light buttons, alpha-numeric keyboards, registers and other software control expedients. The console CRT has a resolution of 1000 lines in 20-inches and the position of any point within the 14-inch by 14-inch centered square can be specified to one tenth of one percent.

The console cabinet is equipped with fixtures to mount the complement of console logic cards required to receive and transmit logic levels, convert digital input to analog signals for deflecting the CRT beam, and to control beam intensity. Two cables of 200-foot maximum length, each consisting of 29 twisted wire pairs serve to interface the display console with the Digigraphic Controller. At the console, 57 twisted pairs are connected to 30 data receivers and 27 data transmitters through 2 connectors. Twenty-four data receivers relay two groups of 12 digital logic levels, one 12-bit group for X coordinates and one for Y coordinates. (Refer to Figure 2-4.) These digital logic levels are decoded, converted to analog signals, and amplified to drive the CRT X and Y deflection coils. Five receivers convey the digital levels required to control beam intensity (bright, medium, and dim) and beam on/off. A single data receiver is used to relay a sample-and-hold clock pulse which maintains analog current levels during changes in digital beam driving signals thereby preventing transients from effecting beam movement.

Attached to the console is a manually operated keyboard (Figure 2-5) consisting of 25 keys; 22 of these keys can be manually latched in the operated position. The other three are used as momentary switches; two of the three are wired in parallel to produce the same result. The console senses the operation of any one of these switches and generates a signal called Delta Keyboard. This Delta Keyboard signal is normally used to flag the program informing it that the keyboard needs servicing. The keyboard action requests are transmitted to the Digigraphic Controller by 24 separate status lines each driven by a single data transmitter. One key on the keyboard,which is designated light pen key (LP) operates in parallel with the switch on the light pen. This allows the operator to enable the light pen fiber optics via the program from either the light pen switch on the light pen or the LP key on the keyboard. A separate transmitter is provided to relay the light pen signal to the controller.

A power interrupt signal, when generated by the console error detec-

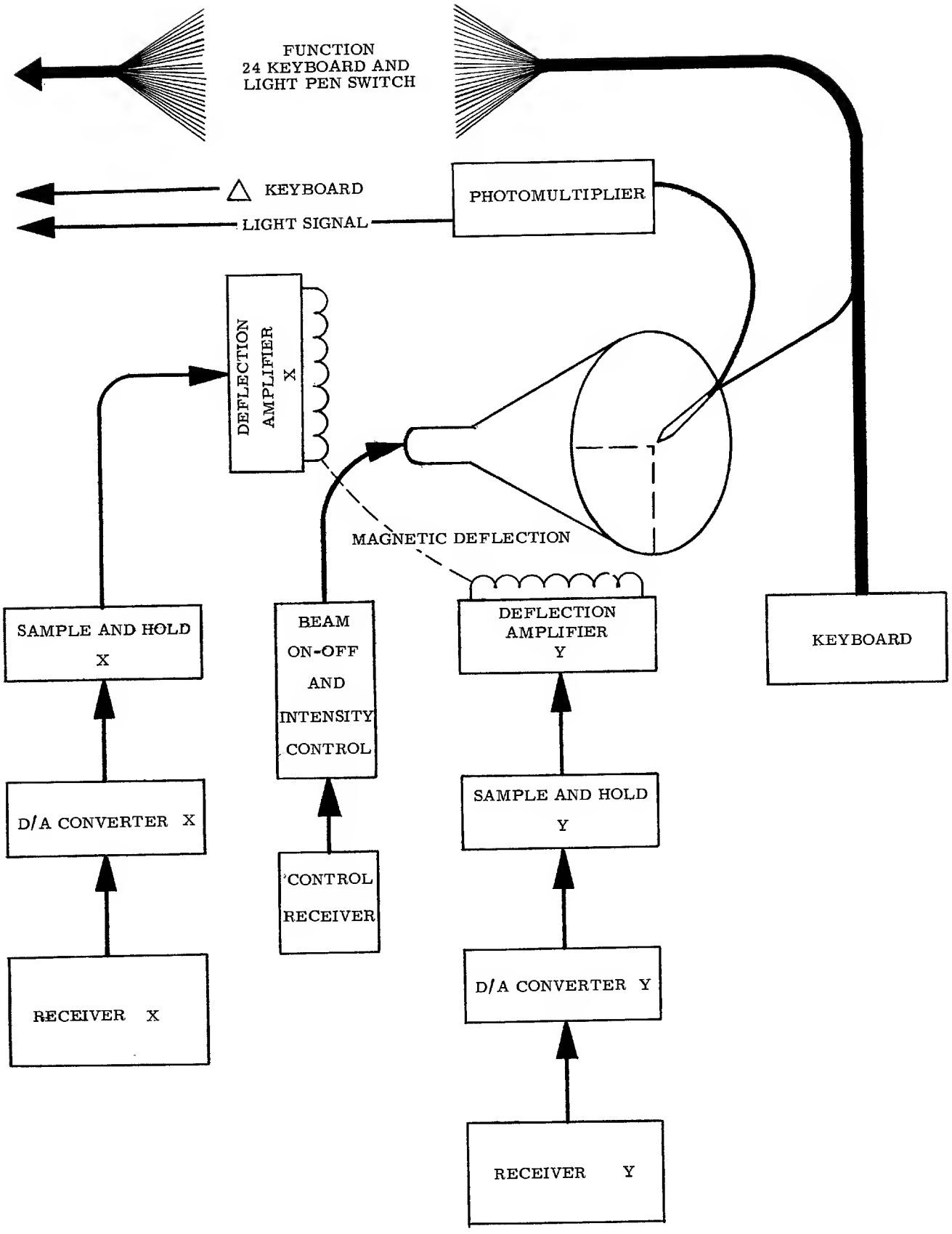


Figure 2-4 Digigraphic Console Block Diagram

tion circuitry, is transmitted by a separate transmitter to the controller for relay to the central computer.

The console cabinet houses two power supplies: a low voltage supply to power console logic cards, the CRT heater and grid, and drive the deflection amplifiers; and a high voltage supply which powers the CRT screen grid, focusing electrode, and anode.

BLOCK DIAGRAM DISCUSSION

Figure 2-6 presents a simplified block diagram of the Digigraphic System showing the major transfer paths for display data and status data within the Digigraphic Controller. Two basic routes are used for transferring display data from the 3200 Computer to an addressed console. The principal route involves the buffer memory, because, in most system uses, display data is initially written onto the drum to provide off-line storage for display programs. This system design feature permits processing of display programs from the buffer memory (drum display) while leaving the computer free for other activities. The other route involved in transferring display data circumvents the drum memory and is used when displaying from computer core memory (core display). For either intended purpose (drum or core display) display data from the 3200 Computer is initially fed across the 3207 interface circuits to the E-Register circuits. From here, data to be displayed from drum memory is written onto the drum via any one of six addressable head bands. Once a display program has been stored on the drum, the head band (used to write the display data onto the drum) may be assigned to any one of the three consoles.

As Figure 2-6 shows, routing of display data from the drum can be made to any one of three Transmission Selector and Control Groups. Each of these three circuit groups correlates directly to one of the three consoles. That is, all display data generating an image on Console No. 1 is routed through Transmission Selector and Control Group No. 1. Display data generating an image on Console No. 2 is routed through Transmission Selector and Control Group No. 2 etc. This holds true when processing display data originating from either drum memory or core.

Note that Figure 2-6 shows three sets of dashed lines entering the Transmission Selector and Control Groups besides those lines (solid lines)

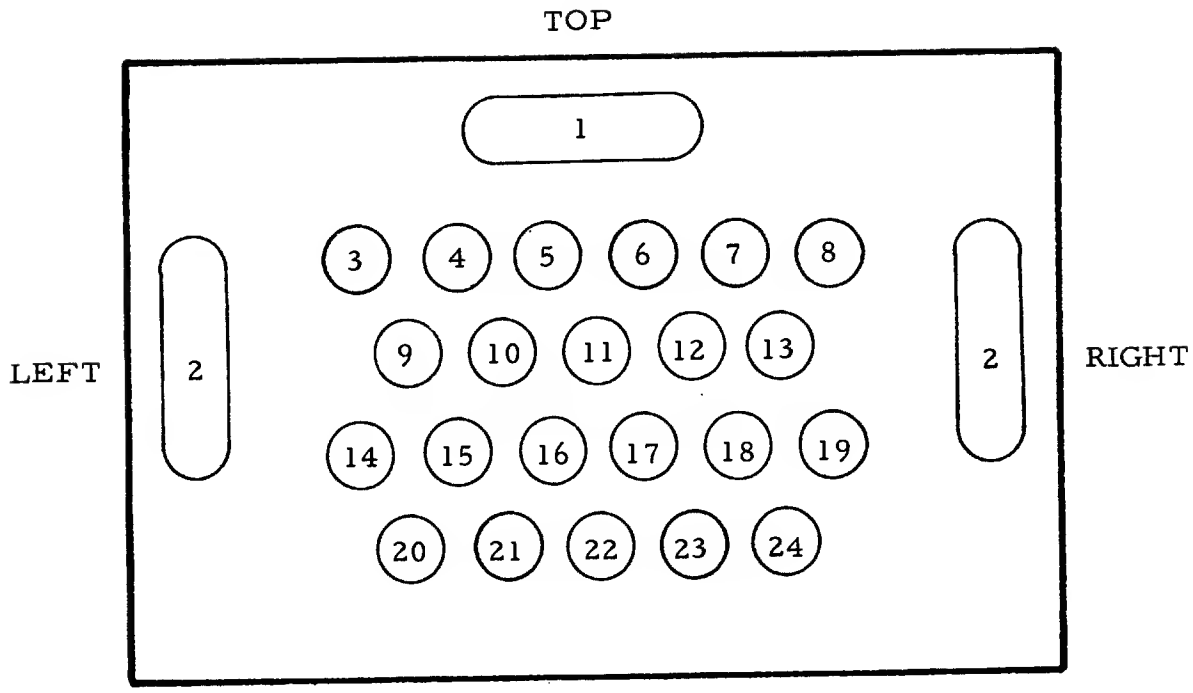


Figure 2-5 Digigraphic Keyboard

that enter from the drum memory. The dashed lines signify the display data transfer path used when displaying from computer core memory.

From the selected Transmission Selector and Control Group, the display data is applied to the X and Y Byte Decoding Circuits. Three time-sharing pulses are shown as being applied to this circuit group, i.e., TS1 through TS3. Additional circuit groups receiving time sharing pulses are the X and Y incrementing circuits and the X and Y Buffer Storage Register Groups for each of the three consoles.

The initial source of all time-sharing pulses is the drum clock pulse which has a frequency of 600KC and a time period of 1.67 usec. Pulses TS1 through TS3 each have a 400 nanosecond time period and they are generated sequentially within the time period of the drum clock pulse.

Since the X and Y Byte Decoding Circuits receive display data inputs from three separate sources, time sharing is required to process the display bytes supplied from Transmission Selector and Control Groups Nos. 1 through 3 within the 1.67 usec. period of the drum clock pulse. Time sharing is such that the first pulse, TS1, strobes the display byte contents of Transmission Selector and Control Group No. 1 through the X and Y Byte Decoding Circuits; the second pulse, TS2, strobes the display byte contents of Transmission Selector and Control Group No. 2 through the X and Y Byte Decoding Circuits, etc.

Each display byte applied to the X and Y Byte Decoding Circuits conveys an X and Y increment value that eventually is used to update the contents of the X and Y Buffer Storage Registers for the associated Console (refer to the Section 3 discussion given on incremental instruction bytes). The task of the X and Y Byte Decoding Circuits is to detect and interpret the sign and increment weight of each display byte being processed. When this activity is completed, the X and Y increment values are fed through the X and Y Incrementing Circuits to update the binary contents of the X and Y Buffer Storage Registers for the associated Console.

NOTE

The above described transfer action is also under time sharing control. That is, a byte processed through the X and Y Decoding Circuits from Trans-

mission Selector Control Group No. 1 is transferred to the X and Y incrementing circuits and then to the X and Y Buffer Storage Register for Console No. 1 before the byte from Transmission Selector and Control Group No. 2 is allowed to enter the X and Y Byte Decoding Circuits.

At any given instant (1.67 usec period) during the processing of a display program the binary contents of the X and Y Buffer Storage Registers specify the last addressed beam position for the associated console. For example, if the binary contents of the Y Buffer Storage Register equal $4020_{(8)}$ and the X Buffer Storage Register contains $0000_{(8)}$ then the addressed position of the beam will be one which defines the beam at the bottom center of the display area. If the next byte processed results in a positive increment being applied to the Y Buffer Storage Register (so that its binary contents are increased) and the binary contents of the X Buffer Storage Register are left unchanged then the beam is deflected upward while remaining centered. Application of a negative increment on the processing of a byte has the opposite effect; that is, the beam is deflected downward. In like manner, positive increments applied to the X Buffer Storage Register causes the beam to be deflected right while negative increments cause it to be deflected left.

Two of the more significant aspects regarding X and Y Buffer Storage Register operation that should be borne in mind are: (1) all bytes making up a display program are processed through these registers 30 times each second and (2) at any given time during the processing of a display program, the instantaneous contents of these registers define the last addressed position of the beam.

All major transfer paths for sending status data back to the computer are shown as either entering or leaving the Interrupt Control and Status Monitoring Circuits. Lines entering these circuits from each of the three consoles convey keyboard and light pen status data. Lines entering from the three X and Y Buffer Storage Register groups convey the last addressed

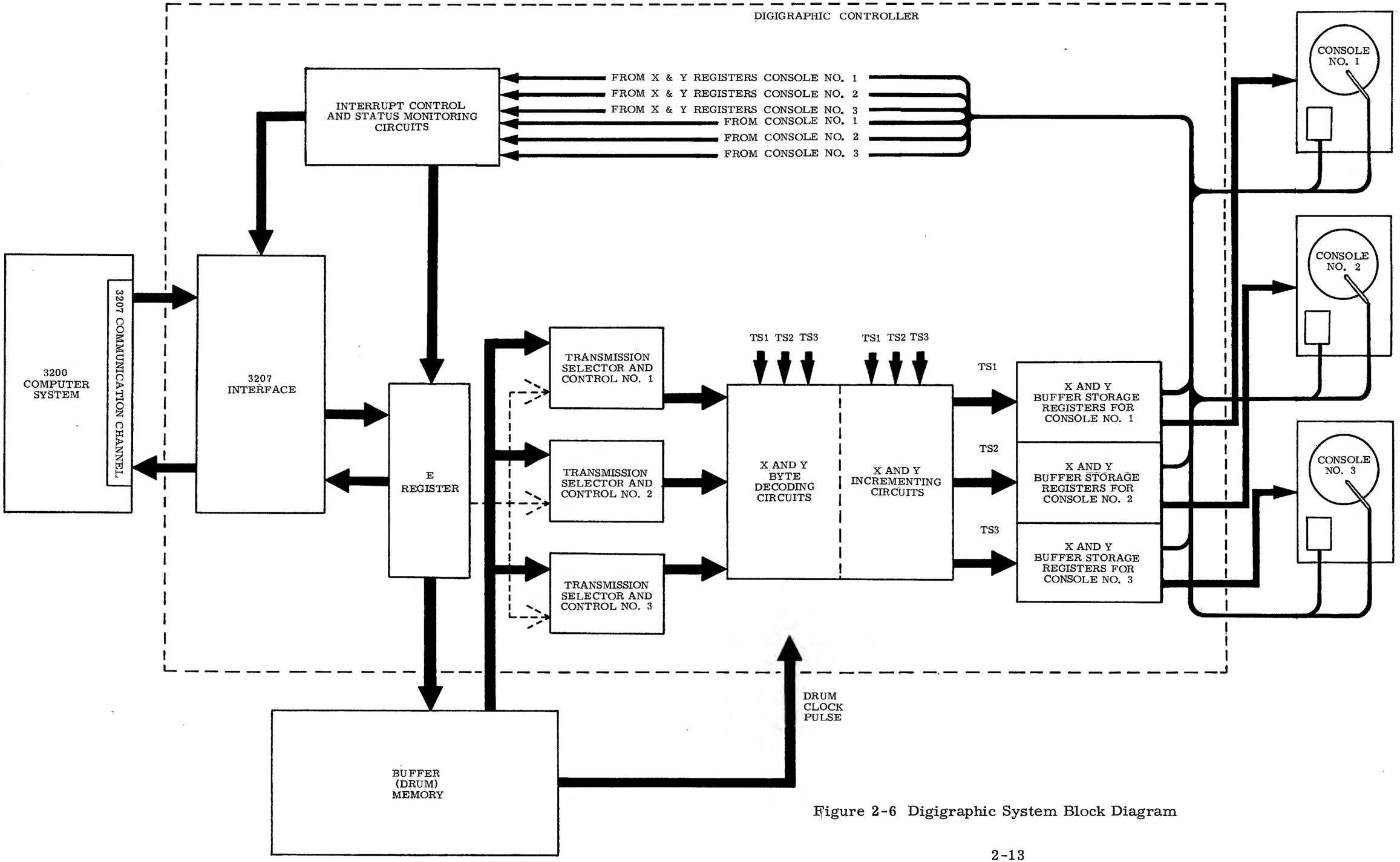


Figure 2-6 Digigraphic System Block Diagram

beam position for the associated console.

The number of status lines entering the Interrupt Control and Status Monitoring Circuits necessitates that there be some control over which status byte is to be transferred and when. For control, a status counter is employed which sequences the transfer of status data through the Interrupt Control and Status Monitoring Circuits.

The transfer path for sending status data back to the 3200 Computer may be through the E register and 3207 Interface circuits in one case or solely through the 3207 interface circuits in the other case. The route chosen depends entirely on computer programming considerations.

GRAPHIC OPERATIONS

Controls: The user has available virtually unlimited controls with which to steer his way through to a solution of a problem or to completion of an assigned task. This seemingly limitless capability is provided not only through the software capabilities utilizing the keyboard, but also through the capabilities built into the software system utilizing the light pen in conjunction with the display CRT.

In general, the keyboard (Figure 2-5) is assigned those functions which are of a general nature or which are performed most often in conjunction with the light pen. All keys may be given new functional assignments through program modification. The lock-down feature of the keyboard not only allows a user to set up what he wants to do deliberately, but also to use keys as mode controls whenever appropriate. The software system has been designed to utilize chording (pressing more than one key at a time) in specifying a process.

The light pen in conjunction with the display is used in a variety of ways in this system. The basic modes are (1) tracking and (2) picking. Each of these may also be broken into modes of useage. Tracking may be used (1) to draw curves in a free hand drawing mode, and (2) to define points, such as center and circumference points for a circle, or the end points of a line. Picking may be used (1) to select a point on a previously defined and currently displayed item as a parameter, (2) to select a previously defined and currently displayed item as a parameter, and (3) to select a displayed light button to initiate some desired process.

It is in this latter mode that the light pen greatly augments the control facilities available to the user. The number of light buttons which may be defined is virtually without limit.

An important feature of this system is the ability to pick a displayed item, whether it be a line or a complicated piece part as a parameter, by selecting appropriate controls and pointing at the item. Once an item has been picked, it may be moved, operated upon, or used in conjunction with other picked items to create the desired model or display or perform a necessary calculation.

Of course, it isn't possible to pick parameters during development of a drawing where no light exists to activate the light pen. In this case it is necessary to pick the tracking cross, which is always shown within the frame, and move it to the desired location for the purpose of defining a point, line parameters, or a reference point.

Free-hand drawing may be performed using the tracking cross and light pen whenever the desired curve is more complex than can be constructed using circles, circular arcs, and line segments, or whenever the inaccuracies of the human hand and eye may be tolerated.

Data Structure: The data structure used in this system to represent user created information allows great flexibility and capacity for the user. The user may construct a model which stays together as he moves it, copies it, etc. He may disassemble, copy, or move a part of it as desired. Or, of course, he may add to or modify parts of it as may be required. Most important of all, (if we call this model an item), it may be grouped with other items to form a more complex or sophisticated model (item).

To reiterate, items (each a model) may be grouped with other items to form a larger model. In turn each is made up of component parts which are in turn items. Further, alphanumeric information may be made a part of a model at any desired level. Any item may have category or reference information defined for it if appropriate (which may be used in searching the structure).

At the bottom of this structure are basic items (called entities) which require a simple definition. These are the graphic entities and alphanumeric entities. The graphic entity types are:

1) Dot
2) Line
3) Circle
4) Arc of a circle, and
5) Polystring

Each of these entities has a standard format descriptor field which defines 1) type of entity, 2) category and reference field, and 3) parental pointer field. The category and reference field may be used as the user deems appropriate. They are intended for use with a classification scheme or an association scheme. The parental pointer provides a means of storing the address of the item (or model) of which it forms a part. This descriptor field may be used to search and select any desired part of a record.

In addition, each has a series of one word quantities which together constitute a data field which stores coordinates in terms of the fixed point construction grid coordinate system.

There is one type of alphanumeric entity. However, four kinds of alphanumeric information may be identified:

1) Text
2) Label
3) Value
4) Notes

The entity type which provides the capability for building properly structured models (items) is called the group entity. The descriptor field is the same as for previously described entities. The data field may contain up to 46 pointers to (addresses of) other entities (the group members). The members of a group can be, of course, graphic, alphanumeric, or group mixed in any quantity (the sum may not exceed 46), or in any order.

Data Display Facility: The display area is classified into two parts: 1) The working surface - generally in the center - enclosed by a frame, and 2) the control surface - the areas which lie outside the working surface.

The working surface provides the graphic display facility of the

Digigraphic System. Two typical working surface sizes are 11 x 17 inches and 14 x 14 inches. One of the features, then, of the working surface is that the frame size may be modified. Other features are zoom control, the tracking cross, and selective display.

The frame size can be specified to be any portion of the display area. One may specify a frame center which is at any point on the display grid, and a frame size (specified by half width and half height) as large or small as desired - rectangular, or square.

Further the user may specify that the frame center be made to coincide with any desired point on the construction grid. This capability allows the user to move his frame around over the construction grid.

The user has complete freedom to specify the amount of magnification desired in viewing the information on the construction grid. He may increase the magnification (increase the zoom index) to observe the detail data in a small effective area of the construction grid space. Or he may decrease the magnification (decrease the zoom index) to observe the gross features over a large effective area of the construction grid space. The user may increase or decrease the zoom index as far as needed to perform his task.

The tracking cross is a permanent part of the display frame. It appears in the upper left hand corner when it is not being used. Use of the tracking cross has been explained previously.

It is likely that as the user works with a model it may be necessary or useful to select certain information for display and for special manipulation, or it may be useful to unclutter the screen to provide temporary working space. For these reasons, this system provides the facility of selecting information for display and for non-display. This selective display in no way affects the information in the data base; that is, all data is available for redisplay.

Control Surface: The area outside the display frame is utilized to display light registers and light button features which were discussed above.

The light registers provide an additional means for the user to input certain special highly formatted alphanumeric information and for the Digigraphic System to communicate certain highly formatted responses.

SOFTWARE SYSTEM

The Function Control Program (FCP) operates as an unstacked job under control of SCOPE-32. Minor modifications are made to SCOPE-32 by FCP at load time. Under SCOPE-32 Control, the normal Control Data I/O procedures apply. FCP is read from the SCOPE-32 Library Tape by a specialized loading routine. Execution control is then transferred to the Resident Executive portion of FCP. From this point on, FCP is executed as function-defined sequences of programs extracted from the modular system library. The Function Control Program is organized as shown in Figure 2-7. This figure depicts the Resident Executive as the control center of the Digigraphic Programming System. The Console Operations result in programming calls for developing and acting upon the operational data. The Resident Executive performs both Computer System and Digigraphic System executive functions and provides system time-sharing control. Functional routines are called from the Processing Library, as a result of specific console operations, or by the FCP Application Interface.

Console operations include the steps necessary to activate the system, perform graphic operations, and terminate system activity upon completion of an assignment. All pertinent system controls are physically located on the Display Console. Console operations are summarized as follows:

1. System Initialization, Load System including FCP. This step enables only the Sign-On functions; there is no display.
2. Sign-On. This step is initiated by pressing the ACCEPT Button. A display band is assigned to the console and all keyboard and light buttons are assigned and enabled. The frame, light buttons, and pertinent registers are displayed. At this point operation may begin.
3. General Digigraphic type operations now commence in a real-time man/machine environment.
4. Sign-Off.

At Sign-Off, control is transferred to a termination routine in a reversion to the system initialization state with only the Sign-On function enabled and with no display. At this point, installation defined accounting procedures can be executed.

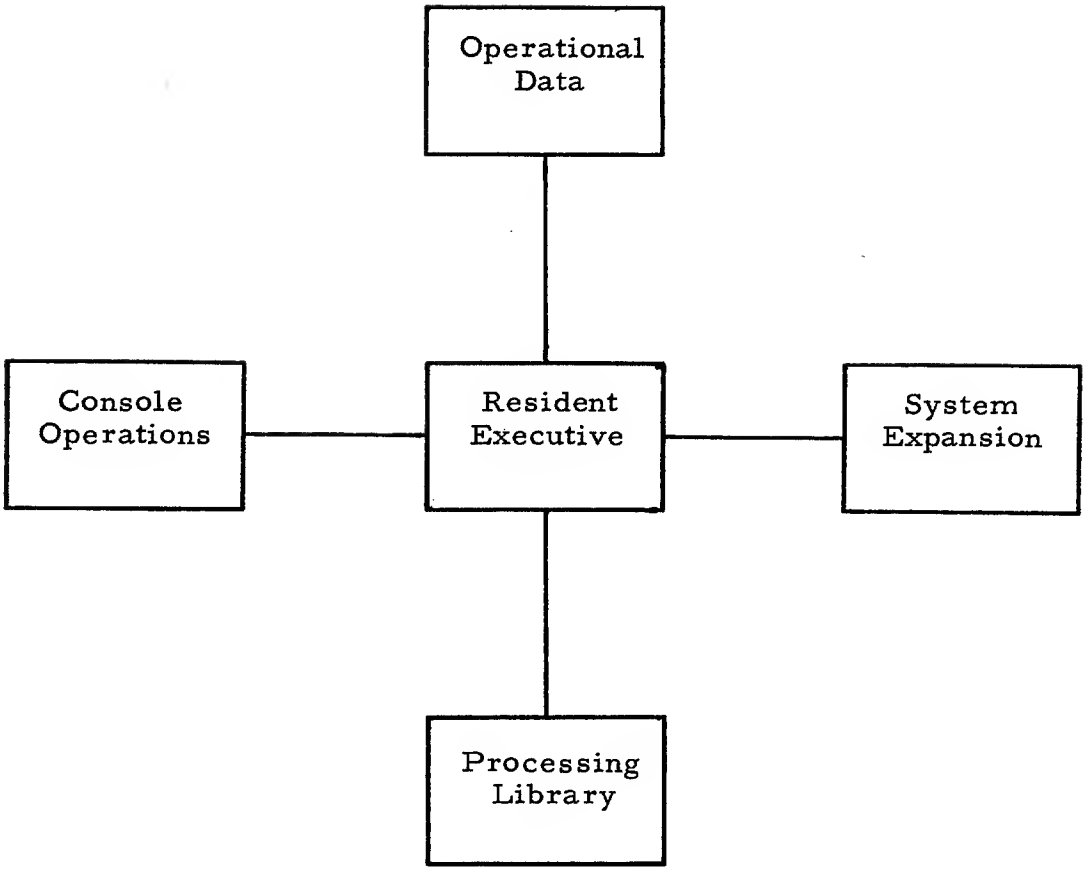


Figure 2-7 FCP Organization

Operational Data: FCP processes four major classes of data, each defined uniquely as to tabular format and data content. These are the Digigraphic List, the Pick Table, the Sequence Table and the Byte List. The Digigraphic List is an ordered centralized tabular output which defines the full extent of the data created and processed by the FCP. The Pick Table stores references to specific parameters selected for subsequent graphic construction or processes by either FCP or Application programs. The Sequence Table stores the processing references for those pertinent control parameters necessary for the execution of FCP and Application Programs. The Byte List is a stream of 12-bit bytes which generate the basic off-line display. These bytes are stored in the display memory. Initially, this byte stream is temporarily call-displayed directly from the Byte List. Upon operator acceptance of the display this byte stream is merged with the related full display on the display Buffer Memory.

Resident Executive: The FCP Resident Executive provides primary control of all system programming functions. This Resident Executive occupies 4500 words in upper and lower main memory and is made up of four distinct sections, namely: the System Monitor, Input/Output Control, the Demand Monitor, and the Sequence Monitor.

The System Monitor is basically the standard SCOPE-32 monitor with minor modifications to permit operation of FCP. Through the system monitor, complete compatibility is maintained with standard 3200 Programming System.

The I/O Control section of the Resident Executive is a collection of I/O routines which because of timing requirements cannot operate under normal SCOPE CIO controls. Operationally these routines perform two overall functions: configuration control, and control of unique input/output equipment.

All Digigraphic System interrupts are processed by the FCP Demand Monitor. The structure of this monitor is such that interrupt lockout is never imposed on the system for more than four milliseconds at a time. The monitor also makes use of display drum lag time by performing those short tasks which can be accomplished without aborting and inhibiting the current task.

Execution of background routines is controlled by the FCP Sequence Monitor during intervals between interrupt processing. Data specifying background routines is obtained by the Sequence Monitor from the Processing Sequence Table.

The FCP Processing Library: All FCP routines with the exception of the Resident are included in the Processing Library. This library is stored in the Buffer Memory as fixed binary ready for loading by the Sequence Monitor.

System Expansion Library: The most important single design aspect of the Digigraphic Programming System is the facility for modular system expansion. The present system expansion includes the Application Interface. As utility programs and utility applications packages are developed they will be added to the system.

In order to accomplish the Application Interface functions provided by FCP, a series of Application Interface routines are defined. These routines operate in conjunction with the FCP to perform those functions for the application which duplicate operator action (Figure 2-8). In addition, several routines are provided to enable the application program to reinterpret and supplement system controls. Call statements of BCD words and numerical parameters establish the conditions for the proper execution of the interface routines. In all cases Application Interface routines are callable as FORTRAN subroutines.

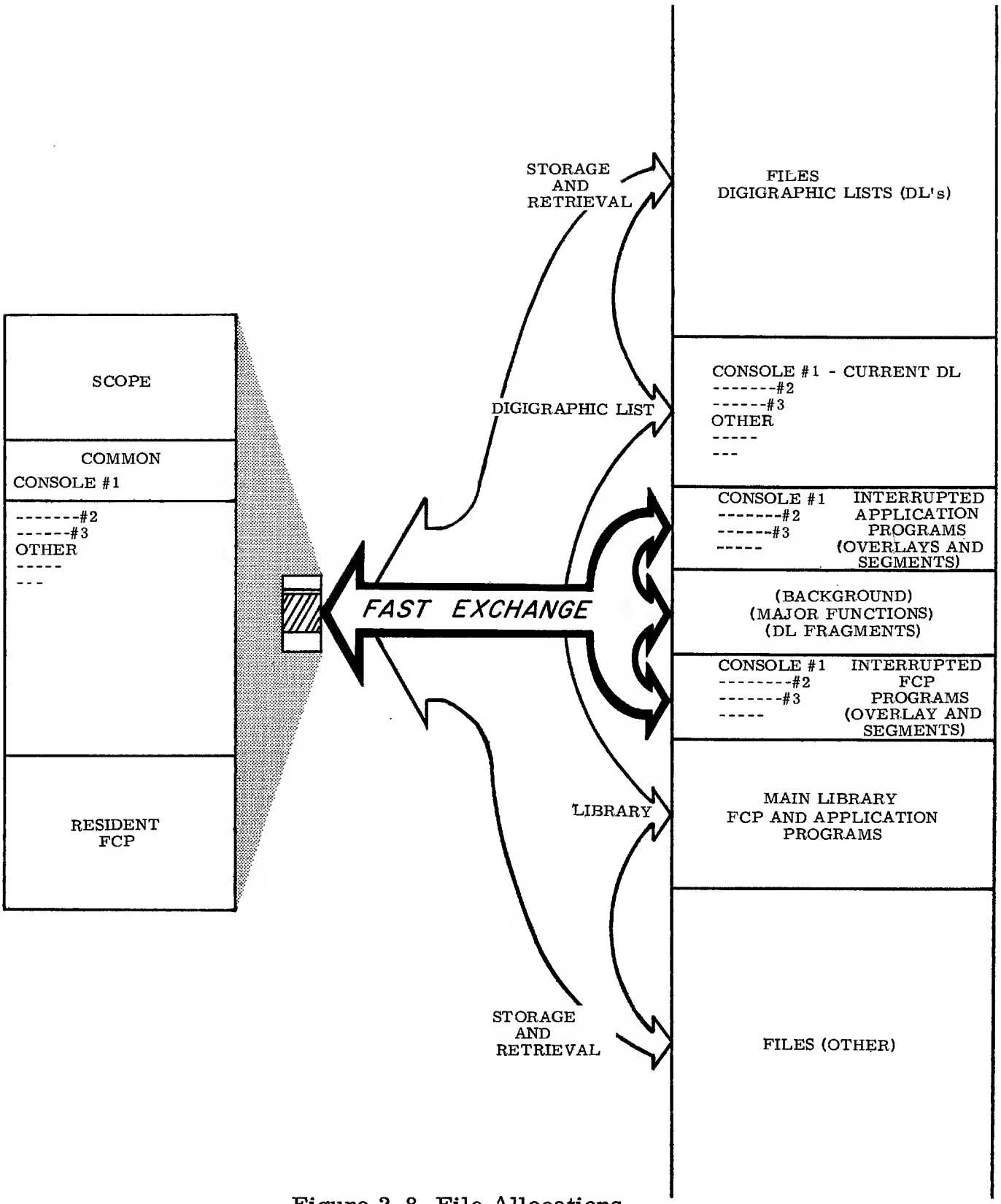
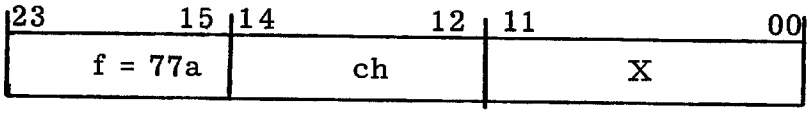


Figure 2-8 File Allocations

SECTION 3
SYSTEM OPERATION

The standard 3200 computer I/O instructions control the exchange of data between the Digigraphic System and the computer. The 3207 communication channel is the communication media for the information exchange (see Figure 3-1). In general, the CON (connect) I/O instruction connects the Digigraphic System to the 3207 communication channel so that subsequent I/O communication is between the Digigraphic System and the computer. The SEL (select) instruction then selects certain functions and operating parameters for the ensuing data transfers. The data transfer instructions (INPW - word-addressed input to storage and OUTW - word-addressed output from storage) may then be given to transfer data. The I/O sense instructions (COPY and EXS) may be used to examine certain parameters within the Digigraphic System.

Although the I/O instructions are described in detail in the 3200 Computer System Reference Manual, for convenience, the sensing and control I/O instruction format will be briefly reviewed here. The format of the sensing and control instruction is shown below. The operation code



for the instruction is 77a, where a refers to the particular I/O instruction; e.g. 770 is the code for the CON instruction and 771 is the code for the SEL instruction. The ch bits shown in the format address the communication channel connected to the computer. Eight communication channels may be connected to the computer. When the communication channel configuration includes a 3207 communication channel, its address is channel 2. Therefore the I/O instructions pertaining to the Digigraphic System contains a 2 for the ch bits. The x bits are used for various control and address functions as explained in the following paragraphs which describe the Digigraphic I/O instructions. For further information on the I/O instructions, refer to the 3200 Computer System Reference Manual.

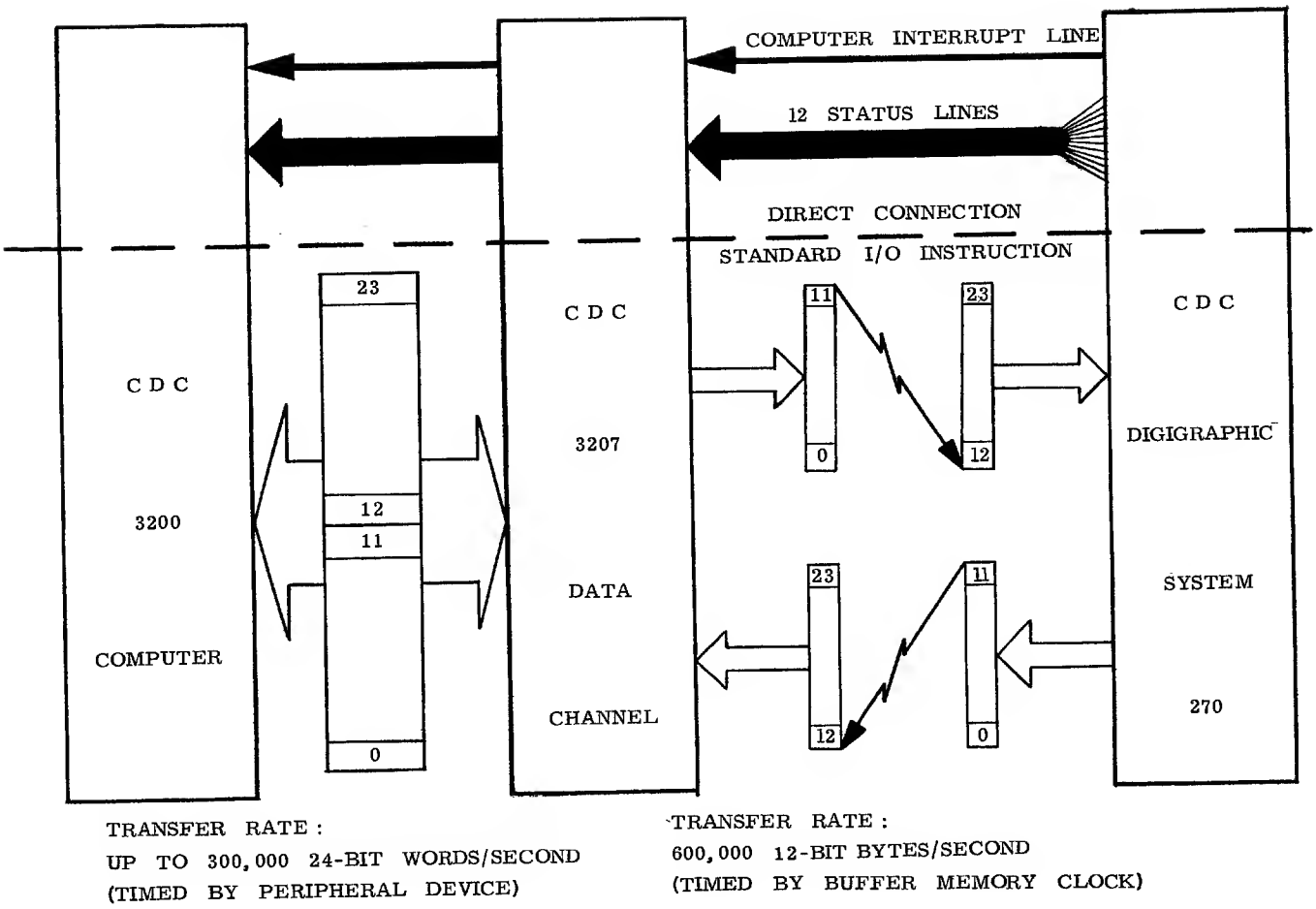


Figure 3-1 Input/Output Communications Link

CONNECT INSTRUCTION

The CON instruction connects the Digigraphic Controller to the 3207 communication channel. Figure 3-2 shows the two possible Digigraphic CON formats; one format addresses the consoles and the other addresses the controller. Bits 23 through 12 of the format were previously explained. Since the 3207 communication channel can accommodate up to eight I/O controllers, bits 11, 10, and 9 are reserved for controller address. The Digigraphic System equipment number (designated DS in format) is 000. Once a CON instruction connects a controller to the 3207 communication channel, all I/O instructions addressing channel 2 (3207 channel) also address the controller connected to the channel.

A reply must be received from the controller following the execution of the CON (or SEL) instruction. When the reply is received by the 3207, the next instruction is read from address P+2. If a reject is received, the channel is busy, or there is no response, a reject instruction is read from address P+1. The reject instruction is normally a jump to a diagnostic or wait routine to enable the program to interpret the cause of the reject and perform the appropriate action.

The UU bits determine which CON format is to be interpreted. When the UU bits contain 00 to address the Digigraphic controller, format 1 is interpreted. Format 1 contains the CL and CM bits which, when 1, clear the logic and the maintenance interrupts, respectively. The LLL bits assign the status array to the status lines so that subsequent sensing instructions sense the LLL-addressed status. For example, if the LLL bits contain 000, the 12-bit status of the controller state is applied to the status lines connected to the 3207 communication channel (connected by the CON instruction). A COPY (copy external status) instruction addressing channel 2 may then be given at any time to transfer the 12-bit status into the computer A register as specified by the COPY instruction. The status configurations are explained later.

When the UU bits address one of the consoles (01, console 1; 10, console 2; and 11, console 3), format 2 is interpreted. The TTT bits contain a drum head band address which, when bit 5 = 1, is assigned to the console addressed by the UU bits. For example, if TTT=001 and UU=01,

CON Format 1 (UU=00)

23 15	14 12	11 9	8	7	6	5	4 2	1 0
f = 770	ch = 2	DS	CL	CM	X	X	LLL	U U

DS = Digigraphic System Address = 000

CL = 1, clear logic interrupts

CM = 1, clear maintenance interrupts

X = Unused

UU = 00 Controller selected

LLL = Selects status as follows:

LLL	
000	Controller State Map
001	Write Buffer
010	Logical interrupt register
011	Maintenance interrupt register
111	No reassignment of status

CON Format 2 (UU=10, 01, or 11)

23 15	14 12	11 10 9	8 7 6	5	4 3 2	1 0
f = 770	ch = 2	DS	TTT	t	LLL	UU

DS = Digigraphic System Address = 000

TTT = Head and TTT assigned to console UU. (TTT = 6 or 7 assigns console UU to core display.)

UU = 01, 10, or 11 selects console 1, 2, and 3 respectively.

LLL = Selects status as follows:

LLL	
000	State Map
001	Byte Buffer
010	X accumulator
011	Y accumulator
100	Upper Keyboard
101	Lower Keyboard
110	Spare
111	No reassignment of Status

t = 1 Assign drum head band (TTT) to console UU

t = 0 No reassignment of TTT

Figure 3-2 CON Instruction Formats

then the data stored on head band 1 is processed by the controller for display on console 1. When bit 5=0, no changes in head band assignments are made. If head band 6 or 7 is addressed the computer takes control of the display for the addressed console; computer control of the display is explained in more detail in later paragraphs.

The LLL bits, as described for the controller, assign a console 12-bit status array to the status lines. The UU bits determine which console supplies the status array.

In general, a single CON instruction suffices for many subsequent I/O instructions if the CON instruction only serves to connect the Digigraphic controller to the 3207 communication channel. Under normal conditions the Digigraphic controller remains connected to the 3207 communication channel. If the I/O instruction requires specification of parameters specified by the CON instruction then, of course, the suitable CON instruction must be given. Note that in one case the CON instruction can stand alone to complete a data transfer; this is when the CON instruction (format 2) assigns a head band to a console.

SELECT INSTRUCTION

The SEL instruction specifies the type and conditions of data transfers, enables and/or disables interrupts, and assigns head bands to consoles. The SEL instruction requires the previous successful execution of a CON instruction. There are two formats for the Digigraphic SEL instruction as shown in Figure 3-3; format 1 pertains to the controller and format 2 pertains to the consoles. The UU bits determine which format is interpreted. When UU=00, format 1 is interpreted; when UU=01, 10, or 11, format 2 is interpreted.

In format 1, the 11, 10, and 9 bits enable or disable the interrupts as shown. It should be noted that the logic interrupts include the light pen, keyboard, and sector pulse interrupts; therefore the logic interrupts must be enabled before a light pen, keyboard, or sector pulse interrupt can be processed. The TTT and SSSS codes specify the head band and sector, respectively, for a subsequent data transfer from the computer which may either write on or read from the specified head band and sector.

SEL Format 1 (UU = 00)

23 15	14 12	11	10	9	8 6	5 2	1 0
f = 771	ch = 2	SP	EL	EM	TTT	SSSS	UU

SP = 1 Enable sector pulse interrupt
= 0 Disable sector pulse interrupt
EL = 1 Enable logic interrupts
= 0 Disable logic interrupts
EM = 1 Enable maintenance interrupts
= 0 Disable maintenance interrupts
TTT = Head band assignment
SSSS = Sector assignment
UU = 00, controller selected

SEL Format 2 (UU = 10, 01, or 11)

23 15	14 12	11	10	9	8 6	5	4 3	2	1 0
f = 771	ch = 2	ED	LP	KB	TTT	t	ab	f	UU

ED	LP	KB	
1	0	1	Enable keyboard interrupt
1	1	0	Enable light pen interrupt
1	1	1	Enable light pen and keyboard interrupt
0	0	1	Disable keyboard interrupt
0	1	0	Disable light pen interrupt
0	1	1	Disable light pen and keyboard interrupt
0	0	0	No effect
1	0	0	No effect

TTT = Head band TTT assigned to console UU. (TTT = 6 and 7 assign console UU to core display)
t = 1 Assign head band TTT to console UU
t = 0 No reassignment of head band TTT
f = 1 Release addressed console from core display
f = 0 No effect
UU = 01, 10, or 11 selects console 1, 2, and 3, respectively
ab = Enables conditions for ensuing input/output data transfer as shown below.

INPW

b \ a	0	1
0	One word Status transfer	ID mode if console is on drum display. X, Y transfer if console on core display.
1	Status map transfer	ID mode if console is on drum display. X, Y transfer if console is on core display.

OUTW

b \ a	0	1
0	Core display, leaves console on core display	Switch console UU to core display. Terminate display on gain of light.
1	Core display, leaves console on drum display	Switch console UU to core display. Terminate display on loss of light.

Figure 3-3 SEL Instruction Formats

In format 2, bits 11, 10, and 9 enable or disable the keyboard and light pen interrupts as shown. When t=1 the TTT bits assign a head band to the UU-addressed console; when t=0, no head band reassignment occurs. (Note that the SEL head band assignment is redundant with the CON instruction - format 2.) The f bit (when 1) releases the addressed console display from computer control. The a and b bits set up conditions for subsequent input/output data transfer as explained in the data transfer paragraphs. Care must be taken when initiating a string of SEL instructions. While each console has separate storage of light pen and keyboard enable or disables and head-band assignment there is only one set of "ab" storage elements for the Digigraphic System. Therefore, "ab" assignment refers to the console last specified and all I/O transfers are directed to or from that console only.

DATA TRANSFER

The INPW and OUTW instructions transfer data between the Digigraphic System and the computer. Before the INPW and OUTW instructions are executed, the CON and SEL instructions must occur to specify parameters for the INPW or OUTW instructions. The CON and SEL instructions also specify whether the communication link is between the computer and the console or the computer and the controller. Each communication link is discussed in the following paragraphs.

Input Word For Controller: A record is read from the drum to the computer from the selected head band beginning with the selected sector. The programming sequence shown below accomplishes this transfer.

Instruction	Address Field Parameters
CON UJP (reject)	Specify channel 2 and DS address=000.
SEL UJP (reject)	Address channel 2 and controller by coding UU=00; select head band and sector by properly coding TTT and SSSS bits.
INPW UJP (reject)	Address channel 2. Specify the initial core memory address and the length of the block transfer. (Refer to the 3200 Computer System Reference Manual).
PAUS UJP (reject)	Channel 2.

Output Word For Controller: A record is written on the drum from the computer to the selected head band and beginning at the selected sector. The programming sequence shown below accomplishes this transfer.

Instruction	Address Field Parameters
CON UJP (reject)	Specify channel 2 and DS address=000.
SEL UJP (reject)	Address channel 2 and controller by coding UU=00; select head band and sector by properly coding TTT and SSSS bits.
OUTW UJP (reject)	Address channel 2. Specify the initial core memory address and length of block transfer. (Refer to the 3200 Computer System Reference Manual for further details.)
PAUS UJP (reject)	Channel 2.

CAUTION: When using the output instructions CON, SEL, INPW, or OUTW, a reject instruction must immediately follow the instruction. For example, the CON instruction is allocated two memory locations, one for the instruction and one for the reject instruction. When the controller sends a reply in response to the CON instruction, the next instruction is read from P+2. If the programmer does not allow for the P+2 jump, the program will be incorrect. It should be noted that COMPASS does not assemble a reject instruction for the specified I/O instruction; the programmer must insert the reject instruction.

Controller Status Transfer: The programming sequence shown below transfers a single status word of the controller to the computer. The controller status words are shown in Figure 3-4 and explained later.

Instruction	Address Field Parameters
CON UJP (reject)	Specify channel 2 and DS=000. Select the desired status by coding the LLL bits and address the controller by coding UU=00.
SEL UJP (reject)	Address channel 2. Select SEL format 2 by inserting a dummy code into UU to address a console. Set ab=00 to select the one-word status transfer.
INPW UJP (reject)	Address channel 2. Select core memory address. Reserve memory space of a one-word transfer.
PAUS UJP (reject)	Channel 2

Status Map Transfer: The complete 16-word status map (Figure 3-4) can be transferred to the computer by the following program.

Instruction	Address Field Parameters
CON UJP (reject)	Address channel 2 and DS=000.
SEL UJP (reject)	Address channel 2. Select format 2 with a dummy console address. Set ab=01 to specify the status map transfer.
INPW UJP (reject)	Address channel 2. Specify the core memory start address. Reserve core memory block for the 24-bit 16-word transfer. (Refer to the 3200 Computer System Reference Manual for further details.)
PAUS UJP (reject)	Channel 2.

Following a status map transfer, the status of the controller state map is applied to the 12 status lines.

Console ID Mode: As an example of this mode, consider the following program.

Instruction	Address Field Parameters
CON UJP (reject)	Address channel 2 and DS=000.
SEL UJP	Select desired console with UU bits. Set ab=10 or 11 to select the ID mode.
INPW UJP (reject)	Address channel 2. Specify the core memory start address. Reserve core memory block for data transfer which includes an undefined number of bytes.
PAUS UJP (reject)	Channel 2.

Assuming that the selected console is on drum display and not locked to core memory display, the above program transfers the identity and coordinates of a displayed graphic interrogated by the light pen. For example, when the light pen is pointed to a displayed graphic and the light pen senses light, the X and Y coordinates of the display are transferred by the INPW as the first word of the data block transfer. The controller continues processing the byte stream from the drum; however, the data transfer does not include non-ID bytes. The first ID byte encountered forms the first byte of the

second word transfer as shown below; the ID bytes that follow are assembled

Word number	Bits 23 through 12	Bits 11 through 00
1	X coordinate	Y coordinate
2	0000 and 8 ID bits, 1st ID	0000 and 8 ID bits, 2nd ID
3	0000 and 8 ID bits, 3rd ID	0000 and 8 ID bits, 4th ID
'		
'		
n	0000 and 8 ID bits, nth ID	Zeroes

into the block transfer as specified by the INPW instruction. When the first non-ID byte occurs, the controller generates an end-of-record signal to terminate the data transfer. This deactivates the channel even though the INPW instruction may have specified more data.

If the end-of-record interrupt was activated for the INPW instruction and the controller initiates the end-of-record, the ensuing interrupt can be cleared only by using the INTS or INCL instruction.

If the console display is locked to the core memory display for the above program, then the X and Y coordinates are transferred to the computer. The X and Y coordinates reflect the coordinates of the last core memory display.

At this point it would be beneficial to elaborate on what is meant when it is stated that a console is on core memory display or controlled by core memory. Ordinarily, the selected head band supplies the byte stream to provide the off-line display. In some instances, however, the computer takes control of a console display and prevents the drum from displaying its byte stream on the display. The instances are:

a. CON or SEL (format 2) instruction assigning drum head band (TTT) 6 or 7.

b. During an OUTW (see SEL format 2) when ab=01 and light pen senses light, or ab=11 and light pen loses light.

c. During an OUTW when ab=00 and the core memory data transfer is complete.

The console display may be released from computer control by executing a SEL instruction (format 2) with bit 2 of the SEL instruction equal to 1.

Output word for Console: For this discussion, consider the following program:

Instruction	Address Field Parameters
CON UJP (reject)	Address channel 2 and DS=000.
SEL UJP (reject)	Select console that is to display core memory data. Select ab=00 mode.
OUTW UJP (reject)	Specify core memory start address. Specify record length.
PAUS UJP (reject)	Channel 2.

The above program permits the core memory display. The computer takes control of the selected console display and inhibits the drum display. The OUTW transfer supplies the byte stream which is processed by the controller for display on the selected console. Since ab=00, at the end of the OUTW block transfer, the core display is terminated, and the console remains under control of the computer.

If ab=01 of the SEL in the above example, the OUTW transfer still supplies the byte stream for core memory display; however, when the OUTW block transfer is complete, the display returns to drum control for off-line drum display.

When ab=10 for the above example, the computer takes control of the selected console and the OUTW transfer supplies the byte stream for core display. If the light pen is activated and it senses light, the core display is terminated when the light pen senses light and the controller ignores the remainder of the OUTW transfer. The X and Y accumulators retain the coordinates of the last core display and the console remains under core display control.

Similarly, when ab=11, the core memory display terminates on loss of light-pen light, the computer retains display control, and the X and Y accumulators contain the coordinates of the last core display.

It should be noted that when the core display is terminated for ab=10 or 11, the INPW instruction can follow to interrogate the coordinates of the last core display.

The controller hardware does not permit a simultaneous core memory display on more than one console. However, multi-console display capability can be accomplished by the software using one of the following techniques:

(1) Write the core display information on a buffer memory head band. When a multi-console display is desired, assign the consoles to this head band and initiate a buffer memory display. This method is advantageous when buffer memory space is not critical.

(2) Simulate simultaneous core display by performing a core display for each individual console at appropriate sector times. If the core displays are about a sector in length (625 words), this can be accomplished by core displaying console 1 at sector 2, console 2 at sector 4, etc. By precessing the sectors, the response time of the display is fast enough to produce a simultaneous core display effect.

(3) Assign multi-consoles to head bands 6 or 7 and initiate a core memory display. Assigning head bands 6 or 7 automatically puts a console on core display.

SYSTEM STATUS INFORMATION AND CONTROL

Status information provides the operational link between the Digigraphic System and the central computer for interpretation of system control and data transfer activities. This information is accessed and routed by the Digigraphic Controller. Status information is modularized to permit transfer of a single 12-bit status array, a 24-bit status word (combined 12-bit status arrays), or a complete 16-word status map. A status map (Figure 3-4) includes four 24-bit words of controller status and four 24-bit status words for each console. Further, the controller and each console can be selectively accessed for specific status information.

There are two methods of status transfer. The first employs the sense I/O instructions - COPY and EXS; the second employs the INPW instruction to transfer a single 12-bit status word or the complete status map. These two methods are demonstrated as follows:

1. Sensing Status - In this method, the CON instruction places the desired status on the status line for inquiry by subsequent sense instructions. The following examples demonstrate this method.

Instruction	Address Field Parameters
CON UJP (reject)	Select channel 2 and DS=000. Select the desired status by properly coding the UU and LLL bits.
COPY	Set bits 00 through 11 = 0000.

In the above example, the selected 12-bit status is loaded into the lower 12 bits of the A-register and the contents of the Interrupt Mask register are loaded into the upper 12 bits of the A-register.

Instruction	Address Field Parameters
CON UJP (reject)	Select channel 2 and DS=000. Select the desired status array by properly coding the UU and LLL bits.
EXS	Set a 1 into the bit position of the desired status of 12-bit status array.

In the above example, the EXS (sense external status) senses the status of the specified bit in the 12-bit status array. If the specified status line is active, the RNI (read next instruction) is at address P+1; RNI at address P+2 if no selected line is active.

2. Status Word Transfer - This method of status transfer was demonstrated previously in the Data Transfer paragraph. However, to emphasize this method, the status word transfers are reiterated in the following examples.

a. Example of one-word status transfer

Instruction	Address Field Parameters
CON UJP (reject)	Select channel 2 and DS=000. Select the desired status array by properly coding the LLL and UU bits.
SEL UJP (reject)	Select SEL format 2 by coding UU=01, 10 or 11. Set ab=00 to select the one-word transfer mode.
INPW UJP (reject)	Specify core memory address and a one-word transfer.
PAUS UJP (reject)	Channel 2.

b. Example of 16-word status map transfer

Instruction	Address Field Parameters
CON UJP (reject)	Select channel 2 and DS=000.
SEL UJP (reject)	Select SEL format 2 with a dummy console address (UU=01, 10 or 11). Set ab=01 to select the status map transfer mode.
INPW UJP (reject)	Specify core memory start address. Reserve a 16-word core memory block.
PAUS UJP (reject)	Channel 2.

Status Map: Figure 3-4 shows the status map which defines the status of the consoles and the controller. This map was discussed earlier during the data transfer and sensing discussion. Figure 3-4 defines the functions of each bit of each byte; however, the following discussion elaborates on each status byte.

Controller State Map: Defines the enabled or disabled states of the light pens and keyboards for each console and the sector pulse. The sector bits indicate the current drum sector address.

Write Buffer: Indicates the current status of the E-register which contains the byte to be written on drum.

Logic Interrupts: Indicate that a light pen, keyboard, or sector pulse interrupt has occurred. Indicates enabled/disabled status of maintenance interrupt. The sector bits indicate the sector at which the first interrupt occurred.

Maintenance Interrupts: Indicate which maintenance interrupt has occurred. The sector bits indicate the current drum sector address.

Console State Map: Defines the termination status of the console display. Indicates whether console is under core or drum display. The TTT bits indicate which drum head band is assigned to that console. The beam-on bit states that the beam is being displayed. The keyboard and light pen levels indicate their activeness.

Byte Buffer: Indicates the current byte being processed.

X coordinate: Indicates the current state of the X coordinate being displayed. If the console is on core display and the display is terminated (i.e. a=1, b=1 or 0 of SEL as described previously) by gain or loss of light-pen light, then the X coordinate contains the X coordinate of the last core

	CONTROLLER OR CONSOLE STATUS REGISTER	STATUS BIT CONFIGURATION OF ASSEMBLED 24-BIT WORD DURING A STATUS MAP TRANSFER												DATA TRANSFER	
		(ODD BYTES)												WORD NO.	BYTE NO.
		23	22	21	20	19	18	17	16	15	14	13	12		
		(EVEN BYTES)													
		11	10	9	8	7	6	5	4	3	2	1	0		
CONTROLLER	CONTROLLER STATE MAP	ENABLED						SECTOR COUNTER				SPE		0	0
		LP3	LP2	LP1	KB3	KB2	KB1								
	WRITE BUFFER	(CURRENT CONTENT OF E REGISTER)												0	1
	LOGIC INTERRUPTS	INTERRUPTS						SECTOR INTERRUPT COUNTER				SPI	MIE	1	2
		LP3	LP2	LP1	KB3	KB2	KB1								
	MAINTENANCE INTERRUPTS	CONSOLE PARITY			CONSOLE POWER			SECTOR COUNTER				CONTROLLER		1	3
		π1	π2	π3	P1	P2	P3					π			
	(NOT USED)	ZEROS												2	4
	(NOT USED)	ZEROS												2	5
	(NOT USED)	ZEROS												3	6
	(NOT USED)	ZEROS												3	7
CONSOLES	CONSOLE 1 STATE MAP	Tc	Pi	Ps	Rxy	T	T	T	Xov	Yov	BEAM ON	KB LVL	LP LVL	4	8
	BYTE BUFFER	(CONTAINS THE CURRENT CONTENTS OF THE BYTE BEING PROCESSED FOR DISPLAY)												4	9
	X COORDINATE	X COORDINATES OF LAST DISPLAY												5	10
	Y COORDINATE	Y COORDINATES OF LAST DISPLAY												5	11
	LEFT KEYBOARD	LEFT KEYBOARD STATUS (KEYS 24 THROUGH 13)												6	12
	RIGHT KEYBOARD	RIGHT KEYBOARD STATUS (KEYS 12 THROUGH 1)												6	13
	(NOT USED)	ZEROS												7	14
	(NOT USED)	ZEROS												7	15
	CONSOLE 2 STATE MAP	Tc	Pi	Ps	Rxy	T	T	T	Xov	Yov	BEAM ON	KB LVL	LP LVL	8	16
	(CONSOLES 2 AND 3 HAVE SAME FORMATS AS CONSOLE 1)													↑ 15	↑ 31

LEGEND: SPE = SECTOR PULSE INTERRUPT ENABLED
LP = LIGHT PEN
KB = KEYBOARD
SPI = SECTOR PULES INTERRUPT
MIE = MAINTENANCE INTERRUPT ENABLED
π = PARITY
P = POWER
Tc = CONSOLE UNDER CORE DISPLAY
Pi = TERMINATE TO INDEX PULSE
Ps = TERMINATE TO SECTOR PULSE
Rxy = TERMINATE TO RESET BYTE
TTT = DRUM HEAD BAND SELECTED
Xov = X OVERFLOW
Yov = Y OVERFLOW

NOTES: (1) A 1 SET INTO A BIT INDICATES CONDITION PRESENT
(2) THE ABOVE SHOWS THE CONFIGURATION FOR A COMPLETE 16-WORD (32-BYTE) STATUS MAP TRANSFER. FOR A ONE WORD TRANSFER, OR WHEN SENSING A STATUS WORD DISREGARD COLUMN 3 AND THE "BYTE" AND "23 THROUGH 12" NOTATION IN COLUMN 2.

Figure 3-4 Status Map Configuration

byte displayed.

Y Coordinate: (same conditions as X coordinate).

Left Keyboard: Indicates the status of keys 13 through 24.

Right Keyboard: Indicates the status of keys 1 through 13.

SYSTEM INTERRUPTS

All Digigraphic System Interrupts are transmitted to the computer over a single interrupt line. A separate interrupt line transmits the standard channel parity error signal. The Digigraphic controller routes an interrupt from the point of origin to the computer. The desired interrupt combination is enabled by the CON and SEL instructions. The EINT (enable) and DINT (disable) computer instructions must be used in conjunction with the CON and SEL instructions.

When an interrupt is enabled, an interrupt is initiated when the enabled condition occurs. The interrupt is identified by a program using the EXS, COPY, or INPW to sense the Digigraphic System interrupt status.

The Digigraphic Interrupts are divided into two classes as follows:

1. Logic Interrupts
   a. Light pen
   b. Keyboard
   c. Sector pulse
2. Maintenance Interrupts
   a. Power failure or transients
   b. Parity error

The following summarizes the light pen interrupt.

1. Condition - Drum display, logic and light pen enabled, and a-bit=1 of SEL format 2.

   Results - Light pen interrupt occurs on gain or loss of light depending on the value of the b-bit in the SEL format. Display uninterrupted.

2. Condition - Drum display, ID mode enabled (SEL format 2, a=1), INPW active and waiting, and light pen interrupt enabled. If conditions not met, light pen strike ignored.

   Results - INPW activated on gain of light. Display uninterrupted.

X, Y coordinates of the light pen strike are transferred as the first word and the following words are made up of the ID bytes.

3. Condition - Core display, light pen interrupt enable not necessary, and SEL format 2 a-bit=1.

Results - Core display terminated on gain or loss (depending on SEL format 2 b value) of light. X and Y coordinates reflect the coordinates of the last core display which is the position of the light pen strike. To reinitiate drum display, a properly coded SEL instruction must be given. To further core display under the same conditions, only an OUTW need be given. Thus an intermix of INPW and OUTW may be given as deemed appropriate by the controlling program.

CONSOLE DISPLAY OPERATION

In the series 270 Digigraphic System, the CRT display is controlled by the display byte stream. The buffer memory supplies the byte stream during off-line buffer display and the computer core memory supplies the byte stream during on-line core memory display. Figure 3-5 shows an example of how the byte stream constructs a display. As shown in Figure 3-5 each vector (incremental) byte moves the beam to construct the A-B display. The beam-off byte turns off the beam so that the beam is not seen when resetting. The reset byte sequence moves to point C to construct the C-D display. Time is required for the beam to stabilize at point C. During stabilization time, ID bytes are given. The ID bytes may be used to identify the previous A-B displayed graphic.

Figure 3-6 shows the CRT grid coordinate addresses in X and Y. A 12-bit X and a 12-bit Y accumulator positions the beam in X and Y, respectively. Hence a grid mesh of 4095 X 4095 addressable locations exists about the CRT; however, some locations are outside the CRT perimeter. The CRT is 20 inches in diameter; therefore, the spacing between each grid is approximately 0.005 inches (20/4095). The beam can be positioned at any one of the 4095 X 4095 locations using the reset byte and the incremental bytes. The following paragraphs summarize the structure of each type of byte.

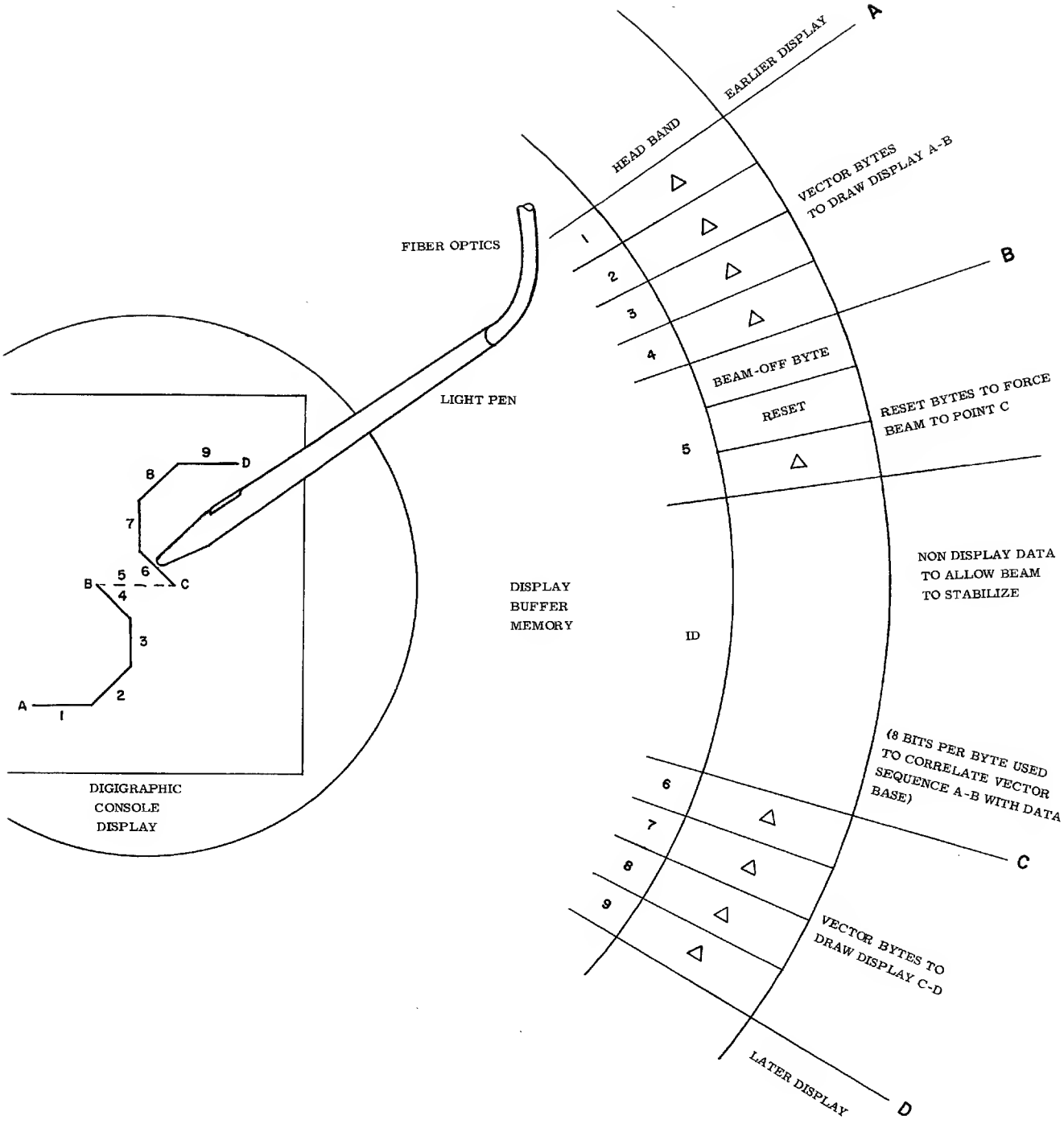


Figure 3-5 Byte Stream Display

Reset Byte: The reset byte is usually the first byte in any series. It is a positioning byte which moves the CRT beam to an approximate position on the display surface. Reset bytes are usually followed by incremental bytes within the byte series to establish the precise point for display initiation. (Refer to Appendix D).

The format for the Reset Byte is as follows:

11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	X	X	X	X	Y	Y	Y	Y

When bits 11, 10, 9, 8 = 1000, a reset byte is designated and bits 7, 6, 5, 4 are jammed into the high order positions of the X-accumulator with the remaining bits set equal to zero. Bits 3, 2, 1, 0 are jammed into the high order positions of the Y-accumulator with the remaining bits set equal to zero. If the sign bit is 1 the value bits are in 1's complement form. The reset byte has no control over the beam on/off state and will follow the beam on/off state of the previous byte.

Identification Byte: The identification byte has an 8-bit identification parameter (ID) in the byte stream. These parameters may be used in identifying displayed graphics. For example, in the Digigraphic Function Control Program (FCP), they contain the Digigraphic List Address of the preceding entity.

Special hardware facilities exist to read these bytes. The ID Mode, as explained in the Data Transfer paragraph, terminates on the last identification byte. Therefore, the system permits the user to vary the number of successive ID bytes to meet the operational requirements.

The format for the identification byte is as follows:

11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	X	X	X	X	X	X	X	X

When bits 11, 10, 9, 8 = 0000, an identification byte is designated. Bits 7 through 0 may contain the previous displayed stream's identification parameter which can serve as a cross indexing facility.

Incremental Byte: The incremental byte is the primary beam moving control byte. In normal operation, an initializing reset byte is used for coarse positioning of a displayed graphic. With the beam off, incremen-

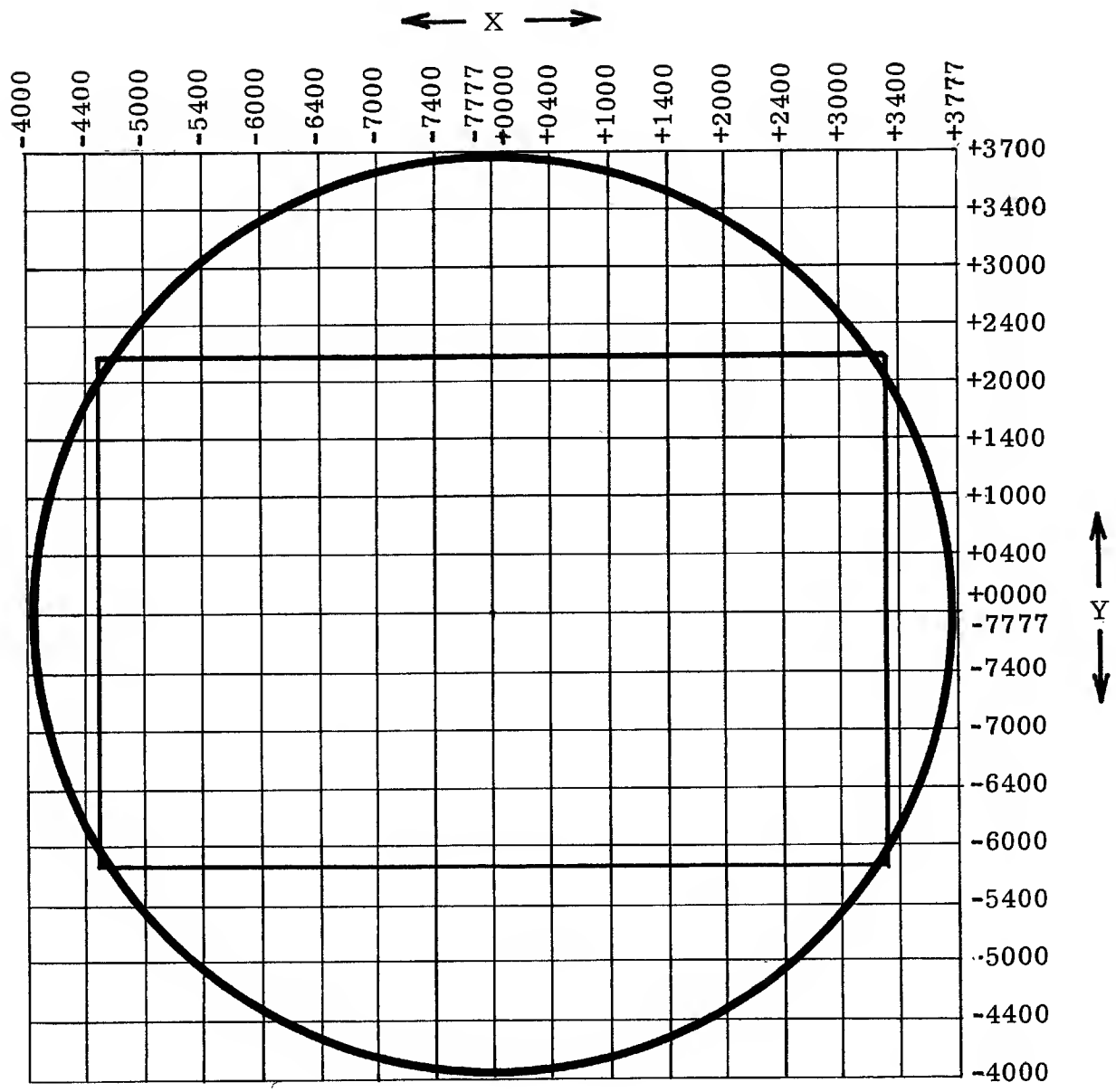
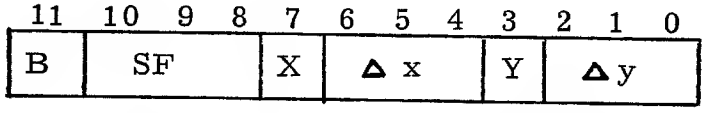


Figure 3-6 X and Y Coordinates

tal bytes establish the precise display starting point (followed by an intensity byte if a change of intensity is desired). Once the desired starting point is established, incremental bytes, the first of which turns the beam on, display the desired graphic.

The format for the incremental byte is as follows:



Bit 11 (B) is the beam control bit; 0 = beam off, 1 = beam on

Bits 10, 9, 8 are binary weighted scale factors (delta multipliers)

SF = 7, 32:1 = .16 inch
= 6, 16:1 = .08 inch
= 5, 8:1 = .04 inch
= 4, 4:1 = .02 inch
= 3, 2:1 = .01 inch
= 2, 1:1 = .005 inch

} per 1 unit in Δx or Δy.

Bit 7 is the X sign bit and bits 6, 5, 4 are the Δx value.

Bit 3 is the Y sign bit and bits 2, 1, 0 are the Δy value.

A scale factor of 2 (1:1) indicates that the 3-bit Δx and Δy are added to the least significant bits of the X and Y accumulators, respectively. A scale factor of 3 (2:1) indicates that the 3-bit Δx and Δy are displaced one bit position to the left of the least significant bit in their respective accumulators and then added; hence a multiplication of 2 or a scale factor of 2:1. Similarly each succeeding scale factor (4 through 7) becomes a power-of-2 multiplier.

The inch notation beside each scale factor denotes the difference in inches between addressed points on the CRT. For example, when the SF=7 (32:1) and a unity value is in Δx, the incremental byte moves the beam in the x direction from its previous position toward a new position 0.16 inches away. However, during one byte time the beam moves only one-half that distance. If no further incremental bytes are given the beam would eventually arrive at the 0.16 inch destination.

When the sign bit of X or Y is negative, the Δx or Δy bits, respectively, must be given in 1's complement form.

A + 0 in Δx and Δy denotes a point plot, whereby the beam (if turned on) is overly intensified at the addressed point; the beam is automatically turned off when the first non-zero code appears in Δx and Δy. A negative zero in Δx and Δy denotes a normal intensity beam (if beam turned on) and the beam remains on until turned off by additional byte.

Intensity Byte: The intensity byte sets the beam intensity control to one of three possible levels, one-half normal intensity, normal intensity, and twice normal intensity. Once the intensity is established, the intensity level remains set until specifically changed. The intensity byte can include the beam on/off control bit (bit 11), which is interpreted as in incremental bytes.

The format for the intensity byte is as follows:

11	10	9	8	7	6	5	4	3	2	1	0
B	0	0	1	0	0	0	0	0	I	I	I

Bit 11 is the beam control bit: 0 = beam off, 1 = beam on

Bits 2, 1, 0 (III) are the beam intensity control bits

III = 001, one-half normal intensity

= 010, normal intensity

= 100, twice normal intensity

Assignment Byte: The assignment byte assigns specific consoles to specific buffer memory head bands. Three separate operational features are made available through this byte.

1) Any console may be assigned to any head band.
2) Consoles can mutually share the same buffer memory display image by being assigned to the same head band.
3) The effective display capacity (byte stream length) can be increased (but repetition rate decreased), by making one head band act as an extension of another one. Because the assignment byte is in the byte stream and is stored in buffer memory, one head band can in turn switch itself to another band.

It should be realized that the processing of these assignment bytes is performed completely off-line. This feature should not be confused with the on-line assignment capability using the CON and SEL instructions

described earlier. For example, the CON or SEL instruction assigns the initial head band to a console. If within the byte stream from the CON or SEL addressed band, an assignment byte specifies a different head band, then the controller processes the newly assigned head band for console display starting at the next sector.

The format (octal) for the assignment byte where T = head band (0-5) is as follows:

Console 1	043 T
Console 2	045 T
Console 3	051 T

Termination Byte: The termination byte causes controlled termination of display for a specific console. Termination may be to the next reset byte, to the next sector on the buffer memory, or to the index pulse (sector 0). Termination bytes may be used to selectively exclude display information from designated consoles. When used in conjunction with the assignment bytes, many variations of controlled inter-display communications can be effected. Again, it should be noted that these are off-line controlled capabilities.

The format (octal) for the termination byte where M is the termination parameter is as follows:

Console 1	062 M
Console 2	064 M
Console 3	070 M

M = 1, terminate to next reset byte

M = 2, terminate to next sector

M = 4, terminate to next index pulse (beginning of selected track or sector 0)

The table on the following page contains a summary of the Digigraphic byte structure.

OCTAL	BINARY	DESCRIPTION
0000 thru 0377	0000-------- xxxxxxxx	Identification Byte 8-Bit Identification Byte
0401, 4401 0402, 4402 0404, 4403	B0010---0III " 001 " 010 " 100 B	Intensity Byte Dim Medium (Normal) Bright B = 0, Beam Off B = 1, Beam On
043T 045T 051T	00010---1TTT 001 010 100	Assignment Byte Console 1 Console 2 Console 3 TTT = Head band 0 - 5
062M 064M 070M	00011---0--- 001 010 100 (M)= 001 010 100	Termination Byte Console 1 Console 2 Console 3 Terminate to next Reset Terminate to next Sector Terminate to Index Pulse (beginning of selected track)
1000 - 3777 and 5000 - 7777	Bwww-------- B www X XXX Y YYY	Increment Byte B = 0, Beam Off, B = 1, Beam On =2-7 for scale factors of 1:1, 2:1, 4:1, 8:1, 16:1, and 32:1, respectively Sign of Delta X Delta X Sign of Delta Y Delta Y
4000 thru 4377	1000-------- X XXX Y YYY	Reset Byte Sign of Delta X Delta X Enter sign and Delta into high-order bits of X. Sign of Delta Y Delta Y Enter sign and Delta into high-order bits of Y

APPENDIX A

INSTALLATION

Two distinct sets of environmental conditions govern the installation requirement for the component units making up the Digigraphic System. The Digigraphic Controller and Drum Memory are designed for operation in a computer environment and consequently require a controlled temperature and humidity. The Console(s), on the other hand, are designed for installation in a less stringently controlled environment such as an office area.

Since the Digigraphic Controller and Drum Memory are to be housed in a computer environment, the installation considerations appropriate to the 3200 Computer also apply for these equipments. (Refer to the Control Data manual titled "3000 Series Computer Systems Site Preparation and Installation Manual")

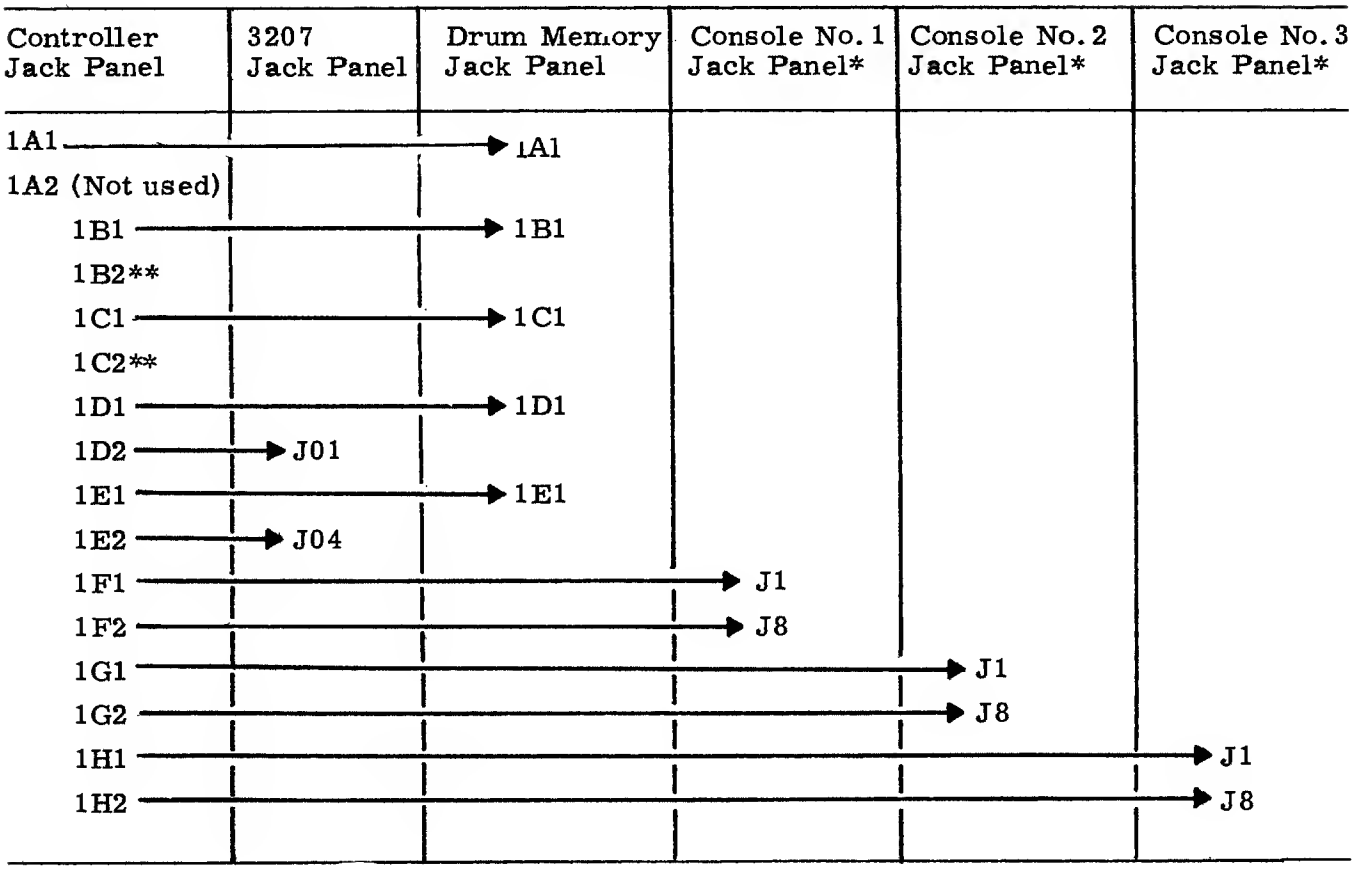
The physical configurations for the Digigraphic Controller, Drum Memory and Console are shown in Figures A-1 through A-3 respectively. Pertinent installation data for each equipment item is summarized in the installation requirements chart. Necessary cabling connections required for tieing the various components of the Digigraphic System together and for connecting the Digigraphic Controller to the 3200 Computer are spelled out in the intercabling connections chart.

DIGIGRAPHIC SYSTEM
INSTALLATION REQUIREMENTS

EQUIPMENT ITEM	DIGIGRAPHIC CONTROLLER	DRUM MEMORY	CONSOLE(S)
Overall Dimensions (in.)	42(W)x20 1/2(D)* x57(H)	48(W)* x30(D)x57(H)	68 7/8(W)x52 1/2(D)x64 1/2(H)
Weight (lbs.)	700	1300	800
Floor Loading	Two parallel bearing bars at 350 lbs. per bar.	Four bearing points at 325 lbs. per point.	Six bearing points at 133 lbs. per point.
Power Service Requirements	208VAC, 3 phase, 400 cps @ 15 amps and 115VAC, 60 cps @ 20 amps.	208VAC, 3 phase, 60 cps @ 15 amps. 208 VAC, 3 phase, 400 cps@ 15 amps	115VAC, 60 cps @ 25 amps.
Heat Dissipation	3000 BTU/hr.	3000BTU/hr.	1600BTU/hr.
Environmental Requirements	Computer Environment	Computer Environment	Normal Office Environment

*Depth of Digigraphic Controller extends to 56 1/2 inches with front and rear doors open; Width of Drum Memory extends to 74 1/2 inches with drum access door open.

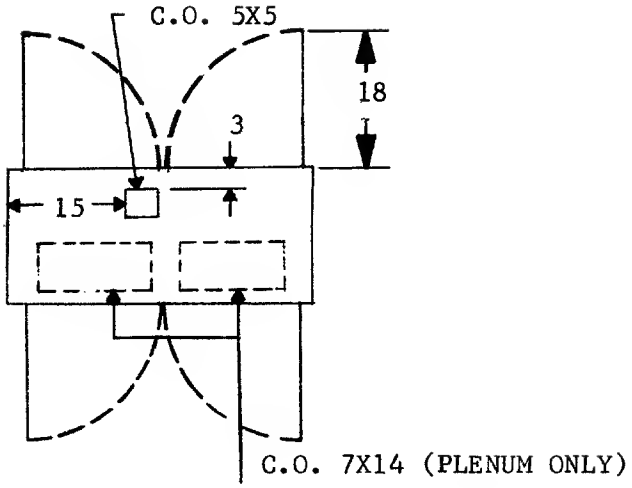
DIGIGRAPHIC SYSTEM
INTERCABLING CONNECTION REQUIREMENTS



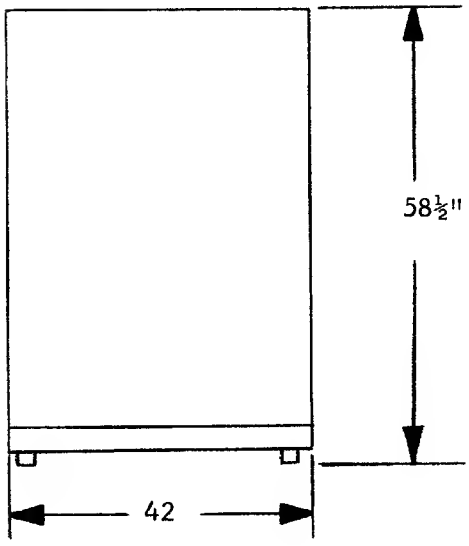
* Two additional cables enter the console jack panel, i.e., the terminator cable and the speaker cable. Both cables are spliced at the Console and enter the jack panel at J7. The terminator cable ties directly to the 3200 Computer main frame terminator power supply. The 3200 source connection for the speaker cable can vary depending on the desired installation configuration.

** Barrel type terminator.

PLAN VIEW



FRONT VIEW



END VIEW
(END PANEL REMOVED)

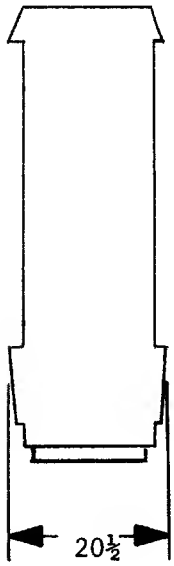


Figure A-1 Controller

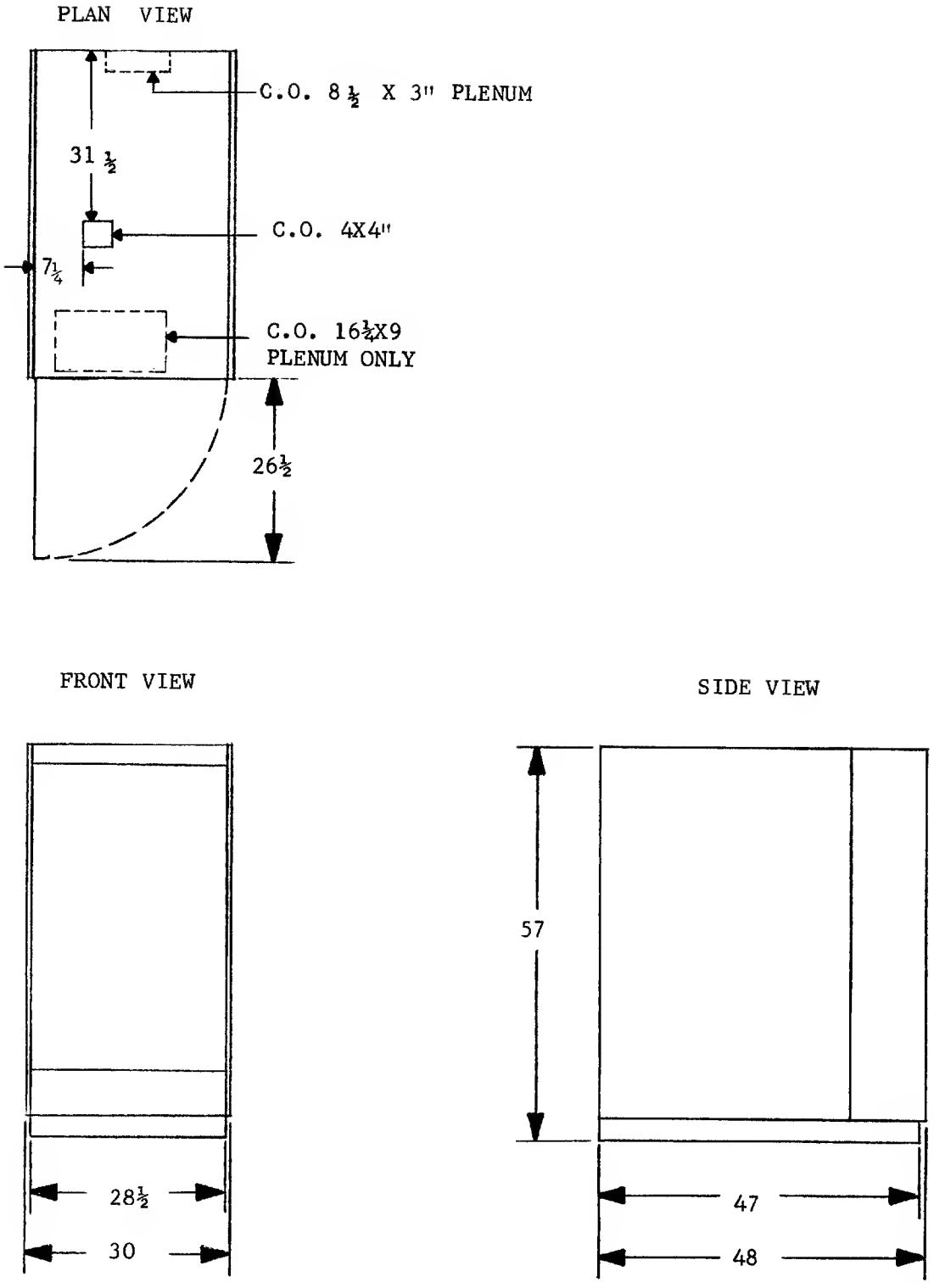


Figure A-2 Buffer Memory

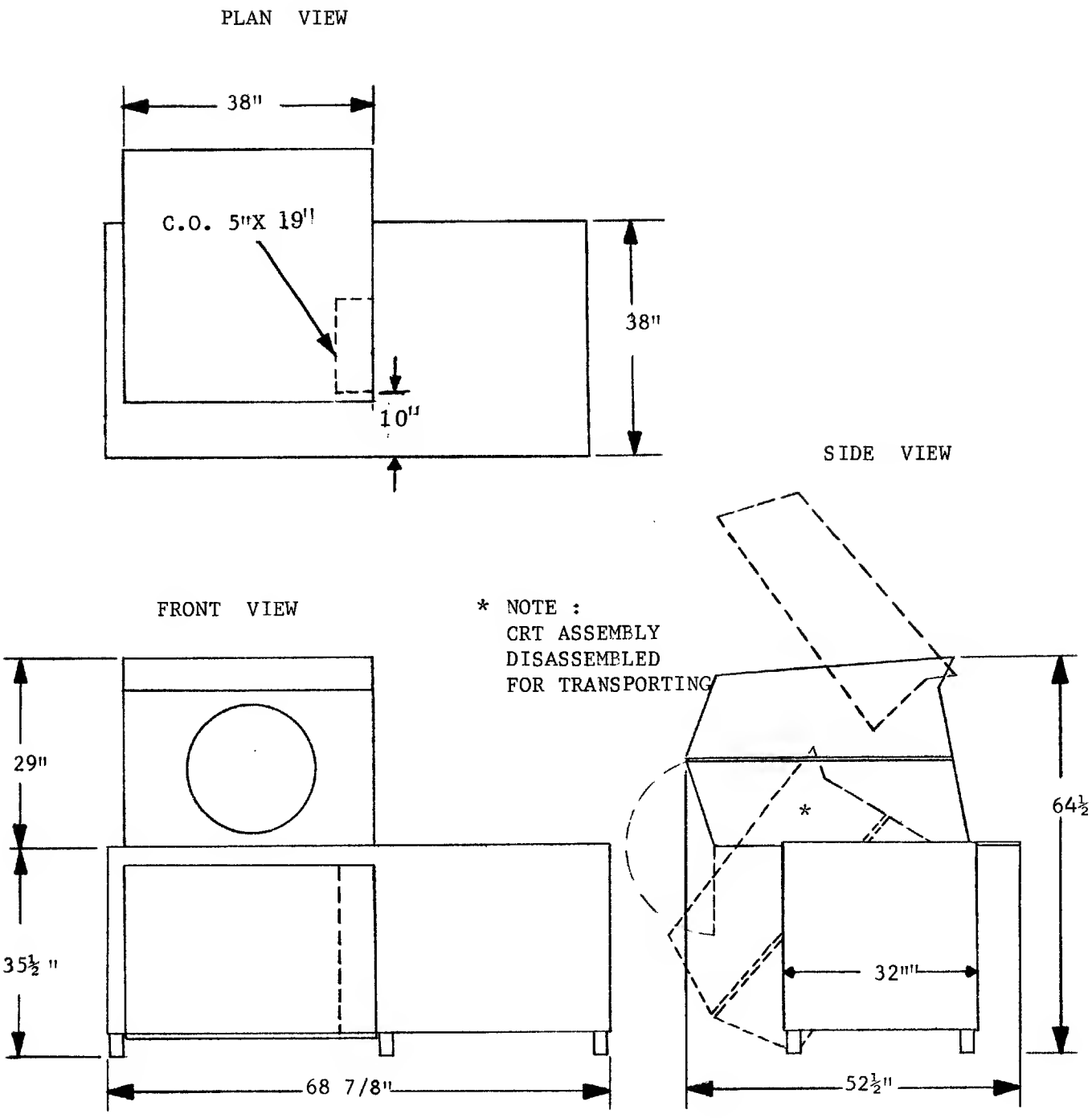


Figure A-3 Console

APPENDIX B

REFERENCE DOCUMENTS

The following documents provide reference material for the Digigraphic System.

Control Data Corporation
3200 Computer System
Reference Manual

Control Data Corporation
3200 Computer System
System Information Manual

Control Data Corporation
3200 Computer System
SCOPE/COMPASS Reference Manual

Control Data Corporation
3200 Computer System
FORTRAN/Reference Manual

Control Data Corporation
3000 Series Computing Systems
Site Preparation and Installation Manual

Control Data Corporation
Digigraphic System 270
Function Control Program Specifications

Control Data Corporation
Digigraphic System 270
Functional Control Program Specifications
Supplement 1, Application Interface-FORTRAN
Subroutine Specifications

APPENDIX C

SUMMARY SPECIFICATIONS

CONTROLLER MODEL 271/BUFFER MODEL 275

Operations	Parallel off-line buffered display processing
	Real-time, time-shared demand interrupt controls
	Core display or Buffer I/O during buffered display
	Executes 600,000 display control bytes/second/console
Commands	Only standard CDC 3200 I/O commands used
	Controller decodes and processes display controls
Data Transfer	Sector-Block Mode, 1250 bytes/block
	600,000 12-bit (plus parity) bytes/second
Storage	120,000 bytes on 6 head bands
	All head bands useable with all consoles (All consoles may share any head group)

DIGIGRAPHIC CONSOLE MODEL 273

- 1 to 3 Consoles per System
- Remote to 1000 feet
- Adjustable CRT tilt 15^{o} to 75^{o}
- Solid-state circuitry throughout
- Over 300 square inches of display surface

Display	Off-line display regeneration, 30 cps.
	22" diameter flat-faced CRT, entire surface addressable in .005" increments
	0.015 - 0.020 spot size at half power points, 3 intensities
	4096 addressable positions in X and Y
	$\pm$ 0.05 inches/8 hours positioning stability
	Point plot or vectors (0.005 to 1.58 inches)
	Constant 1.67 microseconds per display vector
	Point plot time, 25 microseconds maximum
	(9" Circle equals approximately 100 vectors or 167 microseconds).
Light Pen	Pen-shaped with built in pressure switch
	1/8" aperture for tracking and pointing
	48" Fibre optics cord pipes light to detector
Keyboard	25 buttons
	Portable assembly with magnetic grippers
	Symmetrical design with plug for right or left hand operation

APPENDIX D

RESET BYTE TECHNIQUE

This Appendix shows the method employed to reset a display using the reset and the incremental bytes. When bits 11, 10, 9, and 8 = 1000, the reset byte is designated and the four high-order bits of the new X coordinate are jammed into the high-order positions of the X accumulator with the remaining bits set to zero. Similarly, the four high-order bits of the Y coordinate are jammed into the high-order positions of the Y accumulator with the remaining bits set to zero. Subsequent incremental bytes can be used to set the low order bits of the X and Y accumulators. As an example assume that the X coordinate is to be reset to

11 01 10 00 00 00

and the Y coordinate to

00 10 11 10 11 11

This can be done with four bytes: The first is a reset byte; the next three are incremental bytes with scale factors of 32:1, 4:1, and 1:1, respectively. These four bytes are listed below.

	Binary											
	11	10	9	8	7	6	5	4	3	2	1	0
1st byte	1	0	0	0	1	1	0	1	0	0	1	0
2nd byte	0	1	1	1	0	1	0	0	0	1	1	1
3rd byte	0	1	0	0	0	0	0	0	0	0	1	1
4th byte	0	0	1	0	0	0	0	0	0	0	1	1

Note in the 4th byte Bits 2 and 6 are held to zeros so that they will not affect the LSB of the 3rd byte.

The four successive X and Y coordinates generated by the above bytes are shown below.

	Binary													Octal			
1st byte x	1	1	0	1	0	0	0	0	0	0	0	0	=	6	4	0	0
2nd byte x	1	1	0	1	1	0	0	0	0	0	0	0	=	6	6	0	0
3rd byte x	1	1	0	1	1	0	0	0	0	0	0	0	=	6	6	0	0
4th byte x	1	1	0	1	1	0	0	0	0	0	0	0	=	6	6	0	0
1st byte y	0	0	1	0	0	0	0	0	0	0	0	0	=	1	0	0	0
2nd byte y	0	0	1	0	1	1	1	0	0	0	0	0	=	1	3	4	0
3rd byte y	0	0	1	0	1	1	1	0	1	1	0	0	=	1	3	5	4
4th byte y	0	0	1	0	1	1	1	0	1	1	1	1	=	1	3	5	7

The four bytes show a 1 and 3 zeros in position 11. The one appearing in the first byte which is the reset command, has no effect on the beam on/off state. The beam intensity during a reset byte is controlled by the previous byte. The three zeros appearing in the incremental bytes hold the beam off. If the last byte had a one in bits 11, the beam would turn on and the settling trace would be visible to the operator.

If the above method is used, the reset byte always takes the beam to the lower left hand corner of a major coordinate. The remaining bytes will always move the beam up and to the right until it is at its final position. The beam should be allowed 16 byte times (worst case) to come to rest before the beam is turned on.

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